	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	156920	"MAP" or (maximum adj "A" adj posteriori) or turbo or SISO or (modified adj viterbi)	USPAT; EPO; DERWENT	2003/10/28 12:33			0
2	BRS	L2	20271	((look adj up) or lookup) with (entries or index or values or fields or interval)	USPAT	2003/10/28 12:10			0
3	BRS	L3	887	l1 with l2	USPAT	2003/10/28 12:09			0
4	BRS	L4	2448	((look adj up) or lookup) with ((plural$3 or second or two) near4 (entries or index or values or fields or interval))	USPAT	2003/10/28 12:10			0
5	BRS	L5	1457	l1 near4 decod$3	USPAT	2003/10/28 12:11			0
6	BRS	L6	1	l5 with l4	USPAT	2003/10/28 12:11			0
7	BRS	L7	1	l5 same l4	USPAT	2003/10/28 12:11			0
8	BRS	L8	67	l5 and l4	USPAT	2003/10/28 12:11			0
9	BRS	L9	69	l1 with l4	USPAT	2003/10/28 12:14			0
10	BRS	L10	162	l4 with ((comput$5 or calculat$5) near4 (value or data or entr$3))	USPAT	2003/10/28 12:16			0
11	BRS	L11	2	l10 same l1	USPAT	2003/10/28 12:16			0
12	BRS	L12	0	l10 same l5	USPAT	2003/10/28 12:17			0
13	BRS	L13	0	l10 and l5	USPAT	2003/10/28 12:18			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
14	BRS	L14	9	l5 same (table near4 log$7)	USPAT	2003/10/28 12:25			0
15	BRS	L15	0	l5 same (table near4 (log or logaritham))	USPAT	2003/10/28 12:26			0
16	BRS	L16	65	l5 same (log or logaritham)	USPAT	2003/10/28 12:26			0
17	BRS	L17	5	l16 and lookup	USPAT	2003/10/28 12:26			0
18	BRS	L18	28	(l1 near4 decod$3) with (lookup or (look adj up))	USPAT; EPO; DERWENT	2003/10/28 12:34			0

File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200369
(c) 2003 Thomson Derwent

Set	Items	Description
S1	750	(SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIOR? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2	8271	(LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3	80	N(2W)(ENTRY OR ENTRIES)
S4	17327	(SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPL? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADDITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5	38	S2(20N)S3:S4
S6	0	S1 AND S5
S7	917	S2(5N)(SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADDITIONAL)
S8	1	S1 AND S7
S9	28529	(TABLE OR TABLE? ?)(5N)(SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE OR ASSORT? OR ADDITIONAL)
S10	7	S1 AND S9
S11	7	S8 OR S10

11/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06850204 **Image available**
DEVICE AND METHOD FOR CORRECTING AND **DECODING** ERROR OF **TURBO** CODE

PUB. NO.: 2001-077704 [JP 2001077704 A]
PUBLISHED: March 23, 2001 (20010323)
INVENTOR(s): NAKAMURA TAKAHIKO
FUJITA HACHIRO
YOSHIDA HIDEO
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 11-251071 [JP 99251071]
FILED: September 06, 1999 (19990906)
INTL CLASS: H03M-013/29; G06F-011/10; H03M-013/13

ABSTRACT

PROBLEM TO BE SOLVED: To accelerate processing by calculating an average concerning reliability and obtaining soft decision information obtained by correcting the reliability from a ratio of soft decision information of a reception bit to the average so as to correct the soft decision information of each reception bit with a small arithmetic quantity.

SOLUTION: This device has an average calculation means 2 for calculating an average concerning reliability and **decoding soft decision** information calculating means 16 and 17 for obtaining the soft decision information obtained by correcting the reliability from a ratio of the soft decision information of a reception bit to the average. A first dividing means 7 and a first table conversion means 9 constitute the first **decoding soft decision** information calculating means 16 and the second dividing means 8 and the **second table** conversion means 10 constitute the **second decoding soft decision** information calculating means 17. Then, the means 9 and 10 have translation tables obtained by dividing the soft decision information of the reception bit by the average of the reliability to execute conversion to the soft decision information obtained by correcting reliability to be used for decoding with this table.

11/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015404578 **Image available**
WPI Acc No: 2003-466719/200344
XRPX Acc No: N03-371286
LUT (look-up table) addressing scheme for turbo decoding **system involves extracting address bits from index value and using address bits to address** second table
Patent Assignee: SANTOSA H (SANT-I); YUAN W S (YUAN-I); ZHANG M (ZHAN-I)
Inventor: SANTOSA H; YUAN W S; ZHANG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030056167	A1	20030320	US 2001905661	A	20010712	200344	B

Priority Applications (No Type Date): US 2001905661 A 20010712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030056167	A1		19	H03M-013/00	

Abstract (Basic): US 20030056167 A1

NOVELTY - The method entails generating a **second table** having a number of entries based on a first **table** . First and **second** data fields are then generated and an index value is computed. Address bits are extracted from the index value. The address bits are used to

address the **second table** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a circuit for decoding input data; and

(b) a method in a **decoder** applying the **maximum a - posteriori** probability algorithm for computing a specific function for two argument values.

USE - For **turbo decoding** system of communication systems.

ADVANTAGE - Provides improvements to **turbo decoding** that reduces complexity of **turbo decoder** and reduces **decoder** processing time. Applies to LUTs whether scaled or not.

DESCRIPTION OF DRAWING(S) - The figure is a block diagram illustrating a complete iteration of a **decoding** operation of a **turbo decoder** .

pp; 19 DwgNo 3/13

Title Terms: UP; TABLE; ADDRESS; SCHEME; TURBO; DECODE; SYSTEM; EXTRACT; ADDRESS; BIT; INDEX; VALUE; ADDRESS; BIT; ADDRESS; SECOND; TABLE

Derwent Class: T01; U14; U21; W01

International Patent Class (Main): H03M-013/00

File Segment: EPI

11/5/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015269711 **Image available**

WPI Acc No: 2003-330640/200331

XRPX Acc No: N03-264745

Logarithmic functions computing method in digital communication system, involves generating data field including table values computed based on argument equations and scaling table values

Patent Assignee: YUAN W S (YUAN-I)

Inventor: YUAN W S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030014711	A1	20030116	US 2001905568	A	20010712	200331	B

Priority Applications (No Type Date): US 2001905568 A 20010712

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030014711	A1		21	H03M-013/03	

Abstract (Basic): US 20030014711 A1

NOVELTY - A data field including **several table** index values selected from predetermined range of argument values, is generated. The index values are scaled using a scaling factor. Another data field including table values computed based on the logarithmic/natural logarithmic equations involving the argument values, is generated. The computed table values are then scaled by the scaling factor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following.

(1) logarithmic functions computing circuit;

(2) data decoding circuit; and

(3) data receiver.

USE - For computing logarithmic/natural logarithmic functions in data decoding circuits (claimed) in digital communication system and wireless communication system using error correction codes.

ADVANTAGE - The scaling and decoding operations can be performed with greater efficiency.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the **turbo decoder** .

pp; 21 DwgNo 13/13

Title Terms: LOGARITHM; FUNCTION; COMPUTATION; METHOD; DIGITAL; COMMUNICATE ; SYSTEM; GENERATE; DATA; FIELD; TABLE; VALUE; COMPUTATION; BASED; ARGUMENT; EQUATE; SCALE; TABLE; VALUE

Derwent Class: T01; U21; W01

International Patent Class (Main): H03M-013/03
File Segment: EPI

11/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015265238 **Image available**
WPI Acc No: 2003-326167/200331
Apparatus for calculating llr using non-linear look-up table in cdma-2000 mobile communication system
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: LEE J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002093329	A	20021216	KR 200132041	A	20010608	200331	B

Priority Applications (No Type Date): KR 200132041 A 20010608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002093329	A		1	H04B-007/216	

Abstract (Basic): KR 2002093329 A
NOVELTY - An apparatus for calculating an LLR(Log Likelihood Ratio) using a non-linear **look - up table** in a CDMA(Code Division **Multiple** Access)-2000 mobile communication system is provided to improve an error correction performance by calculating the LLR using the non-linear look-up table in a **turbo decoder** .
DETAILED DESCRIPTION - A demodulator(500) demodulates received data. A **MAP** (**Maximum A Posteriori**) **decoder** (600) corrects the signal demodulated in the demodulator(500). The **MAP decoder** (600) has a branch matrix calculator for calculating a branch matrix from the signal demodulated in the demodulator(500), and a backward/forward state matrix calculator for calculating a backward/forward state matrix from the demodulated signal through the branch matrix calculator. The **MAP decoder** (600) has an LLR calculator for comparing the branch matrix calculating value and the backward/forward state matrix calculating value with a non-linear look-up table, and calculating an LLR.
pp; 1 DwgNo 1/10
Title Terms: APPARATUS; CALCULATE; NON; LINEAR; UP; TABLE; CDMA; MOBILE; COMMUNICATE; SYSTEM
Derwent Class: W02
International Patent Class (Main): H04B-007/216
File Segment: EPI

11/5/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014585568
WPI Acc No: 2002-406272/200244
XRPX Acc No: N02-318930
Method and decoder **for** decoding turbo **code**
Patent Assignee: HUAWEI TECH CO LTD (HUAW-N)
Inventor: HU B; SU N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1338824	A	20020306	CN 2000119622	A	20000817	200244	B

Priority Applications (No Type Date): CN 2000119622 A 20000817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CN 1338824	A			H03M-013/00	

Abstract (Basic): CN 1338824 A

NOVELTY - A **decode** method for **Turbo** code features that in the soft input/soft output decode procedure, a decode method based on the maximal posterior probability is used, where a cycle redundancy check code issued to obtain frame error rate, and according to the frame error rate, **several** search **tables** correspondent to the channels (one for one) are used. Its advantages are high decode performance and high robustness.

DwgNo 0/0

Title Terms: METHOD; DECODE; DECODE; TURBO; CODE
Derwent Class: U21
International Patent Class (Main): H03M-013/00
International Patent Class (Additional): H03M-013/23
File Segment: EPI

11/5/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011861979 **Image available**
WPI Acc No: 1998-278889/199825
XRPX Acc No: N98-219797

Decoded **multicolour digital image bit** map **storage method for DRAM used in digital video transmission - involves using colour reference tables for lines and pixels reducing size of bit maps by making two pixels share same colour**

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: NGAI C H
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10093992	A	19980410	JP 97105523	A	19970423	199825	B
US 5784055	A	19980721	US 96643651	A	19960506	199836	
KR 97078500	A	19971212	KR 9710092	A	19970324	199850	
KR 264639	B1	20000901	KR 9710092	A	19970324	200134	

Priority Applications (No Type Date): US 96643651 A 19960506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10093992	A		8	H04N-011/04	
US 5784055	A			G09G-005/06	
KR 97078500	A			H04N-005/445	
KR 264639	B1			H04N-005/445	

Abstract (Basic): JP 10093992 A

The method involves using colour reference tables. Each line of the reference **table** has 8 bytes **table** . **Two** of these bytes are allocated for a control field.

To reduce the size of the bit map, two pixels share the same colour. A bit map is stored in the line corresponding to the horizontal line of a pixel. Each line has a group of colour reference tables.

USE - For broadcast, cable communication, digital network signals, in HDTV, interactive TV, multimedia, VOD, video conference systems and in digital video recording. In standalone units like set top box, digital TV receiver, PC, workstation. ADVANTAGE - Avoids transmission loss.

Dwg.2/8

Title Terms: DECODE; MULTICOLOUR; DIGITAL; IMAGE; BIT; MAP; STORAGE; METHOD ; DRAM; DIGITAL; VIDEO; TRANSMISSION; COLOUR; REFERENCE; TABLE; LINE; PIXEL; REDUCE; SIZE; BIT; MAP; TWO; PIXEL; SHARE; COLOUR
Derwent Class: P85; W04
International Patent Class (Main): G09G-005/06; H04N-005/445; H04N-011/04
International Patent Class (Additional): G09G-005/00; G09G-005/36; H04N-007/24
File Segment: EPI; EngPI

11/5/7 (Item 6 from file: 350)

008727517 **Image available**
WPI Acc No: 1991-231532/199132
XRPX Acc No: N91-176513

Soft - decision - decoding **block code error pattern generator - includes monitor of input syndrome before and after subtraction of address of least reliable data symbol**

Patent Assignee: SIEMENS AG (SIEI)
Inventor: FRIEDERICHS K; FRIEDERICH K J

Number of Countries: 017 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 439649	A	19910807	EP 90101825	A	19900130	199132	B
AU 9170065	A	19910801				199138	
NO 9100357	A	19910731				199140	
FI 9100422	A	19910731				199141	
BR 9100358	A	19911022				199147	
EP 439649	B1	19950705	EP 90101825	A	19900130	199531	
DE 59009376	G	19950810	DE 509376	A	19900130	199537	
			EP 90101825	A	19900130		
FI 100149	B1	19970930	FI 91422	A	19910129	199745	

Priority Applications (No Type Date): EP 90101825 A 19900130
Cited Patents: 6.Jnl.Ref; EP 147623; GB 2185367; JP 60116229; US 4573155; US 4821268; US 4890286
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 439649	A				
	Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE				
EP 439649	B1	G	10	H03M-013/00	
	Designated States (Regional): CH DE GB IT LI NL				
DE 59009376	G			H03M-013/00	Based on patent EP 439649
FI 100149	B1			H03M-013/00	Previous Publ. patent FI 9100422

Abstract (Basic): EP 439649 A

The possible transmission error estimate (syndrome, S) produced from the hard-decision component of each received data block undergoes two subtractions (8,9), of the least reliable symbol address (Sz) from a table (13), and of a partial syndrome (Sy) from a switching network (15) controlled by a counter (14).

The syndrome pairs (Sx, Sy) are tabled (11,12) and output as address combinations (Ax, Ay) along with that (Az) of the least reliable symbol. The monitor (7) controls the switching (10) of the first subtracted address (Sz).

USE/ADVANTAGE - In e.g. digital radio direction-finding. Combinatorial logic computes error patterns simply from syndrome and least reliable symbol address. (8pp Dwg.No. 2/4)

Title Terms: SOFT; DECIDE; DECODE; BLOCK; CODE; ERROR; PATTERN; GENERATOR; MONITOR; INPUT; SYNDROME; AFTER; SUBTRACT; ADDRESS; RELIABILITY; DATA; SYMBOL
Derwent Class: U21; W06
International Patent Class (Main): H03M-013/00
International Patent Class (Additional): H03M-013/00
File Segment: EPI

```
File 348:EUROPEAN PATENTS 1978-2003/Oct W03
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20031023,UT=20031016
         (c) 2003 WIPO/Univentio

Set     Items   Description
S1       1978   (SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-
            R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2      26399   (LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3       1053   N(2W)(ENTRY OR ENTRIES)
S4      29282   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
            ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
            OR ASSORT? OR ADDITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5        336   S2(20N)S3:S4
S6         14   S1 AND S5
S7       4796   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
            ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
            OR ASSORT? OR ADDITIONAL)(5N)S2
S8        105   S1 AND S7
S9         28   S1(S)S7 OR S1(100N)S7
S10        21   S9 NOT S6
```

6/3,K/1 **(Item 1 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

01599330
Cascade Map Decoder **and Method**
Kaskaden-Kartendekoder und Verfahren
Methode et decodeur Map **en cascade**
PATENT ASSIGNEE:
Texas Instruments Incorporated, (279078), 7839 Churchill Way, Mail Station 3999, Dallas, Texas 75251, (US), (Applicant designated States: all)
INVENTOR:
Gatherer, Alan, 2105 Bluebonnet Drive, 75082, Richardson, (US)
Wolf, Tod D., 1321 Alto Drive, 75081, Richardson, (US)
LEGAL REPRESENTATIVE:
Holt, Michael et al (50428), Texas Instruments Limited European Patents Department PO Box 5069, Northampton, NN4 7ZE, (GB)
PATENT (CC, No, Kind, Date): EP 1324502 A2 030702 (Basic)
APPLICATION (CC, No, Date): EP 2002102887 021223;
PRIORITY (CC, No, Date): US 32859 011228
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; SI; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO
INTERNATIONAL PATENT CLASS: H03M-013/45; H03M-013/29
ABSTRACT WORD COUNT: 33
NOTE:
Figure number on first page: 1A

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200327	469
SPEC A	(English)	200327	5106
Total word count - document A			5575
Total word count - document B			0
Total word count - documents A + B			5575

Cascade Map Decoder **and Method**
Methode et decodeur Map **en cascade**

...ABSTRACT A2
MAP decoder with cascade architecture. Iterative **Turbo decoders** can use two such cascade **MAP decoders** with feedback in conjunction with interleaver and deinterleaver where the **MAP decoders** generate extrinsic information for iterations.
...SPECIFICATION A2

BACKGROUND OF THE INVENTION

Field of the invention
The invention relates to channel encoding and decoding, and more particularly to interleaved codes such as **turbo** codes with iterative **decoding** and related systems.

Background
Demand for wireless information services via cell phones, personal digital assistants (PDAs), and Internet appliances (IA) plus wireless networking among notebook...

...and Black et al, A Unified Approach to the Viterbi Algorithm State Metric Update for Shift Register Processes, Proc. ICASSP-92 V-629 (1992). Viterbi **decoding** can be applied to **Turbo** codes.
Figure 2b illustrates an iterative **MAP** (**maximum a posteriori** probability) **decoder** consisting of repeated applications of computations based on the trellises of the two constituent convolutional codes and the interleaver of the encoder of Figure 2a. **MAP decoding** is more complex than but provides better performance than Viterbi

decoding. USP 6,023,783 (Divsalar) discloses various **turbo** encoders and **decoders** , and Hagenauer et al, Iterative Decoding of Binary Block and Convolutional Codes, 42 IEEE Tr.Info.Th. 429 (1996) describes the soft iterative **MAP** **decoding** .

SUMMARY OF THE INVENTION

The present invention provides a **MAP** **decoder** with cascade architecture.

This has advantages including preferred embodiments with faster or simpler **turbo** encoding/ **decoding** .

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings are heuristic for clarity.

Figures 1a-1b show preferred embodiment interleavers.

Figures 2a-2g illustrate a **MAP** **decoder** .

Figures 3a-3g, 4, and 5a-5c illustrate preferred embodiment **MAP** **decoders** .

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Overview

Preferred embodiment communication systems incorporate preferred embodiment encoding and **decoding** methods and include **Turbo** code interleavers with output memory partitioned into banks for quasi-parallel read/writes plus **MAP** **decoders** with reduced complexity cascade circuitry. In particular, preferred embodiment interleavers permute data by reading in chunks of data and writing in parallel into banks up...

...the number of banks (and corresponding write circuits), the larger the chunk size and the greater the average number of parallel writes.

Preferred embodiment cascade **MAP** **decoders** allow for reduction in the number of circuits as compared to parallel **MAP** **decoders** by partitioning the states into subsets and performing the computation of a trellis stage one subset at a time. The cascade **MAP** **decoder** may use fewer circuits than the parallel **MAP** **decoder** because the cascade **MAP** **decoder** can use the same circuit for the computations of multiple states.

Preferred embodiment wireless communications systems components, base stations and mobile users, could each include...

...circuits (ASICs), (programmable) digital signal processors (DSP's), and/or other programmable devices with stored programs for control of the preferred embodiment interleavres and cascade **MAP** **decoders** . The base stations and mobile users may also contain analog integrated circuits for amplification of inputs to or outputs from antennas and conversion between analog...to the beginning of the data block.

(2) Compute the index permutations, (pi)(n), (pi)(n+1), ..., (pi)(n+N-1), such as by reading **N** consecutive **entries** from a permutation **lookup** **table** or special circuit;

(3) Send (pi)(n),x(n) to the write circuit of the output memory bank for addresses than include the index (pi...parallel, the N permuted or inverse-permuted index decisions made, and M data allocated for writing to the left data banks; see Figure 1b.

Iterative **MAP** **decoders**

Figures 2a-2g illustrate the 3GPP **turbo** encoder and an iterative **decoder** which includes two **MAP** blocks, an interleaver, a de-interleaver, and feedback for iterations. The preferred embodiments include cascade architectures for the MAP blocks; and may also include preferred...

...pairs of states s',s connected by a transition with uk)) = -1. The sign of L(uk))(vertical bar)y) then provides the hard decision (**decoder** estimate) for uk)).

The **MAP** blocks apply the BCJR algorithm to evaluate the joint probabilities to generate the soft values for uk)). In particular, the joint probabilities may be factored...requires 2(2n) -1) max* blocks (the max* of 2n) inputs may be computed by a pyramid of (2n) -1) 2-input max*

blocks).
Typically **MAP decoders** partition a sequence of received symbols into sliding windows for simpler processing. In the **MAP decoder** of Figure 2c first the beta state metrics for the trellis stages of the first sliding window are generated and stored in the beta state...
Modifications
The preferred embodiments may be varied while retaining one or more of the features of a quasi-parallel interleaver and a cascade architecture for **MAP decoding** .
For example, a **MAP decoder** for a trellis of size 2n+m) can be factored into subsets of size 2n) and use alpha and beta blocks having a cascade architecture...

...CLAIMS A2
1. A **MAP decoder** , comprising:
inputs for receiving symbols;
a forward recursion block coupled to said inputs, said forward recursion block with cascade architecture;
a backward recursion block coupled...

...The decoder of claim 1 or 2, further comprising:
an input for extrinsic information coupled to said forward recursion and backward recursion blocks.
4. A **MAP decoder** , comprising:
inputs for receiving symbols from an encoder with 2n+m) states where n and m are positive integers;
a forward recursion block coupled to...

...of said ACS units includes 1 2-input max* block; and
said output block includes 2(m+1)2n) 2-input max* blocks.
6. A **turbo decoder** , comprising,
a first **MAP decoder** with inputs for receiving symbols and extrinsic information;
a first interleaver coupled to an output of said first **MAP decoder** ;
a second interleaver coupled to said inputs for receiving symbols;
a second **MAP decoder** with inputs coupled to outputs of said first and said second interleavers and to said inputs for receiving symbols;
a deinterleaver coupled to an output of said second **MAP decoder** ; and

a decision unit coupled to said inputs for receiving symbols and outputs of said first **MAP decoder** and of said deinterleaver; wherein said first and said second **MAP decoders** each includes
(i) a forward recursion block, said forward recursion block with cascade architecture;
(ii) a backward recursion block, said backward recursion block with cascade...

...backward recursion block.
7. The decoder of claim 6, wherein:
the output of said deinterleaver couples to said input for extrinsic information of said first **MAP decoder** to provide feedback for iterative operation.

6/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00983606
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (applicant designated states:
AT;BE;CH;DE;FR;GB;IE;IT;LI;NL)
INVENTOR:

Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS6 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, CAM, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucestershire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 891089 A1 990113 (Basic)
APPLICATION (CC, No, Date): EP 98202149 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 953013018)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-019/00; G06F-013/00; G06F-009/38;
ABSTRACT WORD COUNT: 165

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9902	165
SPEC A	(English)	9902	127403
Total word count - document A			127568
Total word count - document B			0
Total word count - documents A + B			127568

...SPECIFICATION strobe;
Figure 53 shows an MPI read timing;
Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory **map** ;
Figure 56 shows a typical **decoder** clock regime;
Figure 57 shows input clock requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit...
buffering means immediately following the system, whereby time spread for video pictures of varying data size can be controlled.
The system may include a spatial **decoder** having a two-wire interface intercon-necting processing stages, the interface enabling serial processing for data and parallel processing for control.
As previously indicated, the...33 blocks (see Figure 14c) group of blocks which is one macroblock high. By doing that, exactly the same counting mechanisms used on the Temporal **Decoder** for counting through the groups of blocks are also used for MPEG.
There is a correspondence In the way that the circuitry is designed between...pictures for visual display in volves the possibility that a desired scrambled picture can be achieved by varying the re-ordering feature of the Temporal **Decoder** .

4. RAM MEMORY **MAP**
The Spatial **Decoder** , Temporal **Decoder** and Video Formatter all use external DRAM. Preferably, the same DRAM is used for all three devices. While all three devices use DRAM, and all...value register 221.
Since the contents of the detect shift register has been identified-as a start code, its contents must be removed from the **two** wire interface to ensure that no further processing takes place using these 3 bytes. The decode register is emptied, and the value decode shift register...1 Spatial Decoder clock signals
The Spatial Decoder has two different (and potentially asynchronous) clock inputs:

A.7.2 Temporal Decoder clock signals
The Temporal **Decoder** has only one clock input

A.7.3 Electrical specifications

A. ...Decoder are reserved for internal test use.

A.9.1.4 JTAG pins for normal operation
See section A.8.1.

A.9.2 Spatial **Decoder** memory **map**
Video demux extended address space Addr. (hex) Bit num. Register Name
Page references 0x00

0x0F7:0not used 0x107:0horiz(underscore)pels
r(underscore)horiz(underscore...

6/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00983604
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane Stichcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, GLoucester GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 891088 A1 990113 (Basic)
EP 891088 B1 010509
APPLICATION (CC, No, Date): EP 98202133 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 269
NOTE:
Figure number on first page: 38

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199902	662
CLAIMS B	(English)	200119	778
CLAIMS B	(German)	200119	770
CLAIMS B	(French)	200119	881
SPEC A	(English)	199902	126651
SPEC B	(English)	200119	120956
Total word count - document A			127332
Total word count - document B			123385
Total word count - documents A + B			250717

...SPECIFICATION the gate. Apparatus for processing a tightly packed and decorrelated digital signal has a barrel shifter and accumulator for unpacking, a Huffman and run length **decoder** , and an inverse DCPM

Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit...a memory in a raster order. The video formatter described hereinafter provides a wide range of output signal combinations.
In the preferred multi-standard video **decoder** embodiment of the present invention, the Spatial Decoder and the Temporal Decoder are required to implement both an MPEG encoded signal and an H.261...

...for the DRAM interface, the inverse modeller 75, the inverse zig-zag 81 and the inverse DCT 83. The standard independent units within the Huffman **decoder** and parser include the ALU 66 and the token formatter 71.
Referring now to Figure 12, the standard-independent units include the DRAM interface 100...encoded pictures for visual display involves the possibility that a desired scrambled picture can be achieved by varying the re-ordering feature of the Temporal **Decoder** .

4. RAM MEMORY **MAP**
The Spatial **Decoder** , Temporal **Decoder** and Video Formatter all use external DRAM. Preferably, the same DRAM is used for all three devices. While all three devices use DRAM, and all...Huffman Decoder for all three standards.
The Index to Data unit 324 performs the second part of the multi-part algorithm. This unit contains a **look up table** that provides the actual Huffman decoded data. Entries in the table are organized based on the **index** numbers generated by the Huffman Decoder.
The ALU 325 implements the remaining parts of the multi-part algorithm. In particular, the ALU handles sign-extension...ability to take the DRAM interface to high impedance is provided to allow other devices to test or use the DRAM controlled by the Spatial **Decoder** (or the Temporal Decoder) when the Spatial Decoder (orthe Temporal **Decoder**) is not in use. It is not intended to allow other devices to share the memory during normal operation.

A.5.12 Refresh
Unless disabled...

...an interval determined by the register, refresh(underscore)interval.
The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 **decoder** (underscore)clock cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface...Decoder are reserved for internal test use.

A.9.1.4 JTAG pins for normal operation
See section A.8.1.

A.9.2 Spatial **Decoder** memory **map**

SECTION A.10 Coded data input
The system in accordance with the present invention, must know what video standard is being input for processing. Thereafter...data (see Table A.15.2 and Table A.15.3). These default tables must be written into the quantization table memory of the Spatial **Decoder** before MPEG **decoding** is possible.
MPEG also allows two "down loaded" quantization tables. One is for use with intra data and the other with non-intra data. The...

6/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00975324
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA

92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucesterhire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 884910 A1 981216 (Basic)
EP 884910 B1 010509
APPLICATION (CC, No, Date): EP 98202132 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 104
NOTE:
Figure number on first page: 76

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199851	498
CLAIMS B	(English)	200119	330
CLAIMS B	(German)	200119	308
CLAIMS B	(French)	200119	382
SPEC A	(English)	199851	126705
SPEC B	(English)	200119	122739
Total word count - document A			127222
Total word count - document B			123759
Total word count - documents A + B			250981

...SPECIFICATION memory map showing a first arrangement of macroblocks;
Figure 14b is a memory map showing a second arrangement of macroblocks;
Figure 14c is a memory **map** showing a further arrangement of macroblocks;
Figure 15 shows a Venn diagram of possible table selection values;
Figure 16 shows the variable length of picture...

...strobe;
Figure 53 shows an MPI read timing;
Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory **map** ;
Figure 56 shows a typical **decoder** clock regime;
Figure 57 shows input clock requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit...Figure 78 shows an overview of JPEG inverse quantization;
Figure 79 shows an overview of MPEG inverse quantization;
Figure 80 shows a quantization table memory **map** ;
Figure 81 shows an overview of JPEG baseline sequential structure;
Figure 82 shows a tokenised JPEG picture;
Figure 83 shows a temporal decoder;
Figure 84...Therefore, from Cycle 4 to Cycle 5, the data D1 is passed from Stage F to the following device, the data D2 is shifted from **secondary** to primary storage in Stage F, but the data D3 in Stage E is not transferred to Stage F. The data D4 and D5 can...The Spatial Decoder of the present invention performs all the required processing within a single picture. This reduces the redundancy within one picture.
The Temporal **Decoder** reduces the redundancy between the subject

7. Multi-Standard Coding
8. Multi-Standard Processing Circuit-2nd Mode of Operation
9. Start Code Detector
10...encoded pictures for visual display involves the possibility that a desired scrambled picture can be achieved by varying the re-ordering feature of the Temporal **Decoder** .

4. RAM MEMORY **MAP**
The Spatial **Decoder** , Temporal **Decoder** and Video Formatter all use external DRAM. Preferably, the same DRAM is used for all three devices. While all three devices use DRAM, and all...In the present invention, time is saved by detecting these in the Huffman Decoder 321, rather than in the Index to Data unit 324.
This **index** number is then passed to the **Index** to Data unit 324. In essence, the **Index** to Data unit is a **look - up table** . In accordance with one aspect of the algorithm, the **look - up table** is little more than the Huffman code table specified by JPEG. Generally, it is in the condensed data format that JPEG specifies for transferring an...Decoder are reserved for internal test use.

A.9.1.4 JTAG pins for normal operation
See section A.8.1.

A.9.2 Spatial **Decoder** memory **map**
Video demux extended address space Addr. (hex) Bit num. Register Name Page references 0x007:0not used 0x0F 0x107:0horiz(underscore)pels r(underscore)horiz(underscore...

6/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00711606
Start code detector for image sequences
Detektor fur den Startcode von Bildsequenzen
Detecteur de code de depart pour sequences d'images
PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucester. GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674443 A2 950927 (Basic)
EP 674443 A3 951213
EP 674443 A3 981223
EP 674443 B1 010509
APPLICATION (CC, No, Date): EP 95301301 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 891089 (EP 98202149)
(EP 98202154)
EP 884910 (EP 98202132)
EP 891088 (EP 98202133)
EP 897244 (EP 98202134)
EP 901286 (EP 98202135)
EP 901287 (EP 98202166)

EP 896473 (EP 98202170)
EP 896474 (EP 98202171)
EP 896476 (EP 98202174)
EP 896475 (EP 98202172)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 102
NOTE:
Figure number on first page: 61

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2897
CLAIMS B	(English)	200119	647
CLAIMS B	(German)	200119	609
CLAIMS B	(French)	200119	752
SPEC A	(English)	EPAB95	128616
SPEC B	(English)	200119	122384
Total word count - document A			131543
Total word count - document B			124392
Total word count - documents A + B			255935

...SPECIFICATION strobe;
Figure 53 shows an MPI read timing;
Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory **map** ;
Figure 56 shows a typical **decoder** clock regime;
Figure 57 shows input clock requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit...tokens may take the form of an interactive metamorphic interfacing token.

The present invention also provides a system for decoding video data, having a Huffman **decoder** , an index to data (ITOD) stage, an arithmetic logic unit (ALU), and a data buffering means immediately following the system, whereby time spread for video...Huffman coded data words as H.261 or MPEG Huffman coded, means operably connected to the Huffman coded data words receiving means for generating an **index** number associated with each JPEG Huffman coded data word received from the Huffman coded data words receiving means, and means for operating a **lookup table** containing a Huffman code table having the format used under the JPEG standard to transmit JPEG Huffman table information, including an input for receiving an...has been chosen here as the width in the present invention it will be appreciated that bits of other lengths may also be used. The **index** -to-tokens converter 234 converts the information to token images using a second **look - up table** (not shown) similar to that given in Table 12-3 of the Users Manual. The token images generated by the index-to-tokens converter 234...

...negation of an insert image is passed as a second input to the second AND gate 281 over a line 283. The output from the **second** AND gate 281 is passed over a line 284 to an input accept latch 285. The output from the input accept latch 285 is passed...encoded pictures for visual display involves the possibility that a desired scrambled picture can be achieved by varying the re-ordering feature of the Temporal **Decoder** .

4. RAM MEMORY **MAP**

The Spatial **Decoder** , Temporal **Decoder** and Video Formatter all use external DRAM. Preferably, the same DRAM is used for all three devices. While all three devices use DRAM, and all...hypothetical DRAM interface which has one write swing buffer and one read swing buffer. Essentially, this is the same as the operation of the Spatial **Decoder** 's DRAM interface. The operation is illustrated in Figure 23.

Figure 23 illustrates that the control interfaces between the address generator 301, the DRAM interface...

...the result of receiving control tokens, or it may merely generate a fixed sequence of addresses (e.g., for the FIFO buffers of the Spatial **Decoder**). The DRAM interface treats the two wire interfaces associated with the address generator 301 in a special way. Instead of keeping the

SECTION A.10 Coded data input

The system in accordance with the present invention, must know what video standard is being input for processing. Thereafter...up conditions and are entirely contained within the buffers managed by the Spatial Decoder. Stream D is still arriving at the input of the Spatial **Decoder** .

Enables for streams B and C are in the queue. So, when stream A is completed B will be able to start immediately. Similarly C...

6/3,K/6 (Item 6 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00711605

Reconfigurable data processing stage
Rekonfigurierbare Datenverarbeitungsstufe
Etage d'operation de donnees reconfigurable

PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol, BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire, GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire, GL11 5PE, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)

PATENT (CC, No, Kind, Date): EP 674446 A2 950927 (Basic)
EP 674446 A3 960814
EP 674446 B1 010801
APPLICATION (CC, No, Date): EP 95301300 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 144
NOTE:
Figure number on first page: 10

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2475
CLAIMS B	(English)	200131	1079
CLAIMS B	(German)	200131	1072
CLAIMS B	(French)	200131	1186
SPEC A	(English)	EPAB95	125236
SPEC B	(English)	200131	121335
Total word count - document A			127738
Total word count - document B			124672
Total word count - documents A + B			252410

...SPECIFICATION A2

INTRODUCTION

The present invention is directed to improvements in methods and apparatus for decompression which operates to decompress and/or **decode** a plurality of differently encoded input signals. The illustrative embodiment chosen for description hereinafter relates to the decoding of a plurality of encoded picture standards...strobe;

Figure 53 shows an MPI read timing;
Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory **map** ;
Figure 56 shows a typical **decoder** clock regime;
Figure 57 shows input clock requirements;
Figure 58 shows the Spatial Decoder;

Figure 59 shows the inputs and outputs of the input circuit...as an input to an inverse discrete cosine transform (IDCT) 83. The output from the IDCT 83 is passed over line 84 to a temporal **decoder** (not shown).

Referring now more particularly to Figure 12, a temporal decoder in accordance with the present invention is shown. A fork 91 receives as... is fifteen bits wide, allowing for parallel transmission of fifteen bits at a time. The value decoder 228 decodes the value image using a first **look - up table** (not shown). A second output from the value decode shift register 230 is passed to the value decoder 228 which passes a flag to an **index** -to-tokens converter 234 over a line 235. The value decoder 228 also passes information to the **index** -to-tokens converter 234 over a line 236. The information is either the data value image or start code index image obtained from the first **look - up table** . The flag indicates which form of information is passed. The line 236 is fifteen bits wide, allowing for parallel transmission of fifteen bits at a... encoded pictures for visual display involves the possibility that a desired scrambled picture can be achieved by varying the re-ordering feature of the Temporal **Decoder** .

4. RAM MEMORY **MAP**

The Spatial **Decoder** , Temporal **Decoder** and Video Formatter all use external DRAM. Preferably, the same DRAM is used for all three devices. While all three devices use DRAM, and all...be written into RAM1 311 until either there is no more data, or RAM1 is full. When RAM1 311 is full, the input side gives **up** control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between **two** asynchronous clock regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the...

12. PREDICTION FILTERS

Referring again to Figures 12, 17, 18, and more particularly to Figure 12, there is shown a block diagram of the Temporal **Decoder** . This includes the prediction filter. The relationship between the prediction filter and the rest of the elements of the temporal decoder is shown in greater...other various physical characteristics are shown with reference to Table 6.6.

17. KEYHOLE ADDRESS LOCATIONS

In the present invention, certain less frequently accessed memory **map** locations have been placed behind keyhole registers. A keyhole register has two registers associated with it. The first register is a keyhole address register and...For example, a 12 bit signed register will be sign extended to fill a 16 bit memory map location (two bytes) A 16 bit memory **map** location holding a 12 bit unsigned integer will return a 0 from its most significant bits.

A.6.4.3 Keyholed address locations

In the...

...SPECIFICATION the relationship between the flag generator, decode index, header generator, extra word generator and output latches;

Figure 23 is a block diagram of the Spatial **Decoder** DRAM interface;

Figure 24 is a block diagram of a write swing buffer;

Figure 25 is a pictorial diagram illustrating prediction data offset from the...

...strobe;

Figure 53 shows an MPI read timing;

Figure 54 shows an MPI write timing;

Figure 55 shows organization of large integers in the memory **map** ;

Figure 56 shows a typical **decoder** clock regime;

Figure 57 shows input clock requirements;

Figure 58 shows the Spatial Decoder;

Figure 59 shows the inputs and outputs of the input circuit...described hereinafter with reference to the DRAM interface. Typically, a single 4 megabyte DRAM is required by each of the Temporal Decoder and the Spatial **Decoder** circuits.

The Spatial **Decoder** of the present invention performs all the required processing within a single picture. This reduces the redundancy within one picture.

The Temporal Decoder reduces the...encoded pictures for visual display

involves the possibility that a desired scrambled picture can be achieved by varying the re-ordering feature of the Temporal **Decoder** .

4. RAM MEMORY **MAP**

The Spatial **Decoder** , Temporal **Decoder** and Video Formatter all use external DRAM. Preferably, the same DRAM is used for all three devices. While all three devices use DRAM, and all...Table 600, it can be seen that a machine sequence(underscore)start signal is generated by the Start Code Detector, as previously described, when it **decodes** any one of the standard signals indicated in Table 600. The Start Code Detector creates sequence(underscore)start, group(underscore)start, sequence(underscore)end, slice...Decoder are reserved for internal test use.

A.9.1.4 JTAG pins for normal operation

See section A.8.1.

A.9.2 Spatial **Decoder** memory **map**

SECTION A.10 Coded data input

The system in accordance with the present invention, must know what video standard is being input for processing. Thereafter...up conditions and are entirely contained within the buffers managed by the Spatial Decoder. Stream D is still arriving at the input of the Spatial **Decoder** .

Enables for streams B and C are in the queue. So, when stream A is ... are raster ordered within a picture. In a non-interleaved scan, the MCU is a single 8x8 block. Again, these are raster organized.

The Spatial **Decoder** can readily **decode** JPEG data containing 1 to 4 different color components. Files describing greater numbers of components can also be decoded. However, some reconfiguration between scans may...

6/3,K/7 (Item 7 from file: 348)

00313521

Method of decoding a binary scan signal.
Verfahren zum Decodieren eines binaren Abtastsignals.
Procede de decodage d'un signal de balayage binaire.

PATENT ASSIGNEE:
Spectra-Physics, Inc. (a Delaware corp.), (1026770), 3333 North First Street, San Jose, California 95134-1995, (US), (applicant designated states: BE;DE;FR;GB;IT;LU;NL;SE)
INVENTOR:
Cherry, Craig Douglas, 3320 Videra Drive, Eugene Oregon 97405, (US)
Taussig, Andrew Peter, 2515 West 22nd Avenue, Eugene Oregon 97405, (US)
Brooks, Michael T., 25112 Territorial Court, Veneta Oregon 97487, (US)
LEGAL REPRESENTATIVE:
Bankes, Stephen Charles Digby et al (47701), BARON & WARREN 18 South End Kensington, London W8 5BU, (GB)

PATENT (CC, No, Kind, Date): EP 304146 A2 890222 (Basic)
EP 304146 A3 890823
APPLICATION (CC, No, Date): EP 88305545 880617;
PRIORITY (CC, No, Date): US 64110 870618
DESIGNATED STATES: BE; DE; FR; GB; IT; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06K-007/14;
ABSTRACT WORD COUNT: 245

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1342
SPEC A	(English)	EPABF1	20014
Total word count - document A			21356
Total word count - document B			0

Total word count - documents A + B 21356

...SPECIFICATION If space pattern isn't one of these four values return; the test failed. Otherwise go to 4.3.16.
4.3.15 Use the **two look up tables**
space **index** (0..15) = 0,3,2,0,1,0,0,0,4,0,0,0,0,0,0,0
bar index(0..31) =
0,0,0...not successful or the decoded character is not an ambiguous character then go to step 9.3.15. Otherwise, use step 9.3.25 to **decode** segment parity **map** with reverse set false. If segment type is ok, then set segment found true and check if segment type is UPC-A right half or ...to get another character. If not successful or the decoded character is not an ambiguous character then return. Otherwise, use step 9.3.25 to **decode** segment parity **map** (with reverse flag false). If segment type not ok return, otherwise set found segment true and check if segment type is UPC-A right half...

...and do step 9.3.10 to check margin. Set fwd decode true. If margin not OK return, otherwise use step 9.3.26 to **decode** segment parity **map** (with reverse flag true). If segment type not ok return, otherwise set found segment true and check if segment is not type UPC-A right...

6/3,K/8 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01045511 **Image available**
SOFT VALUE CALCULATION FOR MULTILEVEL SIGNALS
CALCUL DE VALEUR SOUPLE POUR SIGNAUX MULTI-NIVEAUX
Patent Applicant/Assignee:
TELEFONAKTIEBOLAGET L M ERICSSON (publ), SE- 126 25 Stockholm, SE, SE (Residence), SE (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
WILHELMSSON Leif, Lyftvagen 5, S-240 10 Dalby, SE, SE (Residence), SE (Nationality), (Designated only for: US)
MALM Peter, Annehemsvagen 37, S-226 48 Lund, SE, SE (Residence), SE (Nationality), (Designated only for: US)
Legal Representative:
ZACCO DENMARK A S (agent), Hans Bekkevolds Alle 7, DK-2900 Hellerup, DK,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200375528 A1 20030912 (WO 0375528)
Application: WO 2003EP1945 20030226 (PCT/WO EP0301945)
Priority Application: EP 2002388019 20020307; US 2002363415 20020312
Designated States: AE AG AL AM AT (utility model) AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ (utility model) CZ DE (utility model) DE DK (utility model) DK DM DZ EC EE (utility model) EE ES FI (utility model) FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK (utility model) SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW (EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI SK TR (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW (EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 8938

Fulltext Availability:
Detailed Description
Claims

Detailed Description
... by the dominant contributions to the sums of probabilities in the likelihood ratio (A.J. Viterbi, "An intuitive justification and a simplified implementation of the **MAP** **decoder** for conventional codes",

IEEE Journal on selected areas in communications, 16(2), February 1998). Even though this approximation significantly reduces the computational 1 0 complexity...is identified, thereby providing a computationally very efficient method which eliminates the need of online distance calculations.

Preferably, the stored information is stored in a **look - up table** comprising a **plurality** of pre-computed distance functions **indexed** by the number of signal symbols and the bit positions of the number of bit sequences, thereby providing fast access to the information.

In one...noise. In fig. 2, the cross 201 represents an example of a received signal r.

Prior to providing the received 16QAM radio symbols to a **decoder** , e.g. a **turbo decoder** , they are converted into soft values. Hence, a soft value is calculated

Claim
... according to any one of the claims 1 through 6, characterised in I 0 that the stored pre-computed distance function is stored in a **look - up table** (508; 808) comprising a **plurality** of pre-computed distance functions **indexed** by the number of signal symbols and the bit positions of the number of bit sequences.

8 A method according to any one of the...

6/3,K/9 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00984064 **Image available**
A PRINTING CARTRIDGE WITH SWITCH ARRAY IDENTIFICATION
CARTOUCHE D'IMPRESSION AVEC IDENTIFICATION D'UNE MATRICE DE COMMUTATEURS
Patent Applicant/Assignee:
SILVERBROOK RESEARCH PTY LTD, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SILVERBROOK Kia, Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (Designated only for: US)
Legal Representative:
SILVERBROOK Kia (agent), Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200313860 A1 20030220 (WO 0313860)
Application: WO 2002AU1053 20020806 (PCT/WO AU0201053)
Priority Application: US 2001922029 20010806
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 142964

Fulltext Availability:
Detailed Description

Detailed Description

... lookup is used, although different indexes must be generated and passed into the lookup.

I Dimensional Structures
Direct Lookup
A direct lookup is a simple **indexing** into a I dimensional **lookup table** . Clients can choose between 3 access modes by setting appropriate bits in the Flags register.
Read only
Write only
Read-Modify-Write
Read Onl
A...GetControlData(source, destBlocks, lastBlock))
return error
destBytes = ((destBlocks-1) * destBlockLength) + lastBlock
offsetToNextDuplicate = destBlocks * SOUTCeBlockLength
// Skip the control blocks and position at data
source += numControlBlocks * sourceBlockLength
// **Decode** each of the data blocks, trying
H duplicates as necessary
blocksInError = 0;
for (i=O; i<destBlocks; i++)
found = DecodeBlock(source, dest);
if (! found)
f...to return the values at the specified coordinates in readiness for bilinear interpolation. The basic process is as indicated in Fig.

97 and the following **lookup table** is used.

Lookup Size Details
LU, Image Bilinear Image lookup [X, Y]
width by Table **indexed** by the integer part of X and Y.

Image 4 entries returned from Bilinear index ...N.L
Calculating the dot product of vectors N and L is defined as.

XNXL + YNYL + ZNZL
No bump-map
When there is no bump- **map** N is a constant [0, 0, 1]. N.L therefore reduces to ZL.

With bump-map
When there is a ...the specular contribution where the following constants are set by software.

Constant Value
K, ks
K2 ksc
K3 (I -ksc)lp
I 0 The following **lookup table** is used.

Lookup Size Details
LU, 32 entries X11
16 bits per Table **indexed** by 5 highest bits of integer R*V
entry Result by linear interpolation of 2 entries using fraction of ROV.

Interpolation by 2 Multiplies.

The...

6/3,K/10 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00747344 **Image available**
2-DIMENSIONAL INTERLEAVING APPARATUS AND METHOD
DISPOSITIF ET PROCEDE D'ENTRELACEMENT BIDIMENSIONNEL

Patent Applicant/Assignee:
SAMSUNG ELECTRONICS CO LTD, 416, Maetan-dong, Paldal-gu, Suwon-shi, Kyungki-do 442-370, KR, KR (Residence), KR (Nationality)
Inventor(s):
KIM Beong-Jo, Mujigaemaeul 201 Shinan Apt. #303-804, Kumi-dong, Puntang-gu, Songnam-shi, Kyonggi-do 463-500, KR
KIM Min-Goo, 973-3, Youngtong-dong, Paltal-gu, Suwon-shi, Kyonggi-do 442-470, KR
Legal Representative:
LEE Keon-Joo, Mihwa Bldg. 110-2, Myongryun-dong 4-ga, Chongro-gu, Seoul 110-524, KR
Patent and Priority Information (Country, Number, Date):
Patent: WO 200060752 A1 20001012 (WO 0060752)
Application: WO 2000KR316 20000406 (PCT/WO KR0000316)
Priority Application: KR 9911799 19990406
Designated States: AU BR CA CN IN JP
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Filing Language: English
Fulltext Word Count: 7452

Fulltext Availability:
Detailed Description

Detailed Description
... method for reading data stored at a corresponding address by generating an address at every symbol clock using an index generating rule rather than a **look - up table** method for storing the interleaver **index** .

In conclusion, when **various** interleaver sizes are required and the hardware complexity is restricted in an E
4T-2000 or UMTS system, the turbo interleaver should be designed to...for a given input frame size, performance of the turbo encoder is determined depending on a constraint length K and the proper-ties of the **turbo** interleaver. In designing a **decoder** , the constraint length K is set to 3) or 4 in consideration of the resulting complexity and the desired performance improvement. For example, in CDMA...

6/3,K/11 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00473016 **Image available**
A CAMERA WITH INTERNAL PRINTING SYSTEM
APPAREIL PHOTOGRAPHIQUE A SYSTEME D'IMPRESSION INTERNE
Patent Applicant/Assignee:
SILVERBROOK RESEARCH PTY LIMITED,
SILVERBROOK Kia,
WALMSLEY Simon,
LAPSTUN Paul,
Inventor(s):
SILVERBROOK Kia,
WALMSLEY Simon,
LAPSTUN Paul,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9904368 A1 19990128
Application: WO 98AU544 19980715 (PCT/WO AU9800544)
Priority Application: AU 978003 19970715; AU 978005 19970715; AU 978031 19970715; AU 977991 19970715; AU 977998 19970715; AU 977988 19970715; AU 977993 19970715; AU 978012 19970715; AU 978017 19970715; AU 978014 19970715; AU 978025 19970715; AU 978032 19970715; AU 977999 19970715; AU 978024 19970715; AU 978016 19970715; AU 978030 19970715; AU 977938 19970715; AU 977997 19970715; AU 977979 19970715; AU 978015 19970715; AU 977978 19970715; AU 977982 19970715; AU 977989 19970715; AU 978019 19970715; AU 977980 19970715; AU 977942 19970715; AU 978018 19970715; AU 978021 19970715; AU 978000 19970715; AU 977940 19970715; AU 977939

19970715; AU 978020 19970715; AU 977985 19970715; AU 977987 19970715; AU 978022 19970715; AU 978029 19970715; AU 978023 19970715; AU 978028 19970715; AU 978027 19970715; AU 978026 19970715; AU 977983 19970715; AU 977986 19970715; AU 977981 19970715; AU 977977 19970715; AU 977934 19970715; AU 977990 19970715; AU 978497 19970811; AU 978505 19970811; AU 978498 19970811; AU 978504 19970811; AU 978501 19970811; AU 978500 19970811; AU 978502 19970811; AU 978499 19970811; AU 979395 19970923; AU 979404 19970923; AU 979394 19970923; AU 979396 19970923; AU 979397 19970923; AU 979398 19970923; AU 979399 19970923; AU 979400 19970923; AU 979401 19970923; AU 979402 19970923; AU 979403 19970923; AU 979405 19970923; AU 97959 19971216; AU 981397 19980119; AU 982370 19980316; AU 982371 19980316; AU 984094 19980612
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 191348

Fulltext Availability:
Detailed Description

Detailed Description
... The nUcrocode for the Adder/Logic process block is described in the following table. The interpretations of some bit patterns are deliberately chosen to aid **decoding** . Microcode bit interpretation for Adder/Logie unit
Bits Description
0000 = A+B (carry in = 0)
0001 = A+B (carry in = carry out of previous operation...

6/3,K/12 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00443949
DATA ENCODER/DECODER FOR A HIGH SPEED SERIAL LINK
CODEUR-DECODEUR DE DONNEES POUR LIAISON SERIE HAUTE VITESSE
Patent Applicant/Assignee:
FUJITSU NETWORK COMMUNICATIONS INC,
FUJITSU LIMITED,
Inventor(s):
CALDARA Stephen A,
SLUYSKI Michael,
STROUBLE Raymond L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9834413 A2 19980806
Application: WO 98US1443 19980127 (PCT/WO US9801443)
Priority Application: US 9736617 19970130
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 7413

Fulltext Availability:
Claims

English Abstract
...a ten bit run length limited code for serialization and transmission over the serial data link. A second decoding lookup table is employed at the **decoder** to **map** the received ten bit run length limited code into

the original 8 bit value.

Claim
... the event said DC
balance controller output signal is in said first state.

2 The encoding apparatus of claim 1 wherein said map
comprises a **lookup table** containing said plurality of run
-20
length limited codes as entries within said **table** and said
lookup table is **indexed** by said **plurality** of input values.

3 The encoding apparatus of claim 1 wherein said
conditional inverter is operative to pass the respective run
length limiited code through...The method of claim 15 wherein said
mapping step
comprises the step of mapping said input values into
corresponding run length limited codes in a **lookup table**
indexed by said input values.

17 The method of claim 16 wherein said **lookup table**
comprises a **plurality** of **lookup tables** and said **indexing** step
comprises the step of **indexing** into one of said **plurality** of
lookup tables to access the respective Run length limited
-24 code.

18 The method of claim 16 further comprising the step of
determining whether the Run length...

...a zero.

21 A decoder for converting a plurality of balanced and
imbalanced run length limited codes into a corresponding
plurality of data values, said **decoder** comprising:
a **map** for mapping said plurality of run length limited
codes into said plurality of data values, wherein said map is
operative to provide as an output...produce as an output a
single data value in response to the input of each imbalanced
Run length limited code and its complement.

22 The **decoder** of claim 21 wherein said **map** comprises a
lookup table.

23 The decoder of claim 22 wherein said lookup table is
operative to provide as an output an 8 bit data...

6/3,K/13 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00424651 **Image available**
DOWNLOADING IMAGE GRAPHICS WITH ACCELERATED TEXT CHARACTER AND LINE ART CREATION
PROCEDE DE TELECHARGEMENT DE GRAPHIQUES DE CREATION D'IMAGES AVEC CREATION ACCELEREE DE CARACTERES DE TEXTE ET DE DESSINS AU TRAIT
Patent Applicant/Assignee:
PHILIPS ELECTRONICS N V,
PHILIPS NORDEN AB,
Inventor(s):
VAN DER MEULEN Pieter Sierd,
ROELOFS Gregory R,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9815113 A1 19980409
Application: WO 97IB1027 19970825 (PCT/WO IB9701027)
Priority Application: US 96722415 19961001
Designated States: CN JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Publication Language: English
Fulltext Word Count: 4601

Fulltext Availability:
Detailed Description

Detailed Description
... using, e.g., an N-tap filter, with N typically being larger than 3. The result may be quantized to the original's limited color **map** , if any. **Decoder** 810 may apply dithering methods to the restored background in order to improve the background's appearance on display 808. The feasibility of this option...resolution representation 202 as a first index, and the limited number of possible Y-values for the Ycomponent in high-resolution representation 204 as a **second index** to access a predetermined color- **look - up table** 1102 for direct conversion into combined image 1002 in RGB-format.

This avoids the time-consuming floating-point calculations mentioned above, but is feasible only...

6/3,K/14 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00377046 **Image available**
SYSTEM AND METHOD FOR MULTIPLEXING A SPREAD SPECTRUM COMMUNICATION SYSTEM
SYSTEME ET PROCEDE DE MULTIPLEXAGE D'UN SYSTEME DE COMMUNICATION A SPECTRE ETALE
Patent Applicant/Assignee:
KUMAR Derek D,
Inventor(s):
KUMAR Derek D,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9717789 A1 19970515
Application: WO 96US17993 19961104 (PCT/WO US9617993)
Priority Application: US 95554364 19951106
Designated States: AL AU BB BG BR CA CN CZ EE GE HU IL IS JP KP KR LK LR LT LV MG MK MN MX NO NZ PL RO SG SI SK TR TT UA UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 21455

Fulltext Availability:
Detailed Description

Detailed Description
... correlation sums determined by correlators 17 at the sampling point are reorganized as a serial sequence of sums by parallel-to-serial converter 19. For **soft - decision** maximum likelihood (ML or Viterbi) **decoding** of convolutional error codes, approximately three bits of quantization information is preserved for each correlation sum. For hard 23 decision decoding of ECC codes, only...

...information, beyond the sign bit, for each of the correlation sums provides reliability information that can be used to improve the performance of the Viterbi **soft - decision decoder** . The bits determine an approximate measure of the distance between the correlation sum and the zero value. The zero value is typically the decision-switching...is shown to reduce the effects of gain instability present at the receiver. Uncompensated amplitude variations in the received is signal degrade the effectiveness of **soft - decision** convolutional **decoding** by the Viterbi algorithm, which is

otherwise optimum in a maximum-likelihood sense. According to the method, the effects of gain instability are mitigated by...maximum correlation sum
magnitude. The function is evaluated for all indices. The index corresponding to an indicator value of one is used together with a **table look - up** to determine the encoded value for the selection bits (e. g. **two** -bit values 00 for **index** 1, bit values 01 for index 2, bit values 10 for index 3, and bit values 11 for index 4). A disadvantage of this function...together with the polarity estimates for

10/3,K/1 **(Item 1 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

01424784
SOFT-OUTPUT DECODER
SOFT-OUTPUT DEKODIERER
DECODEUR A SORTIE PONDEREE
PATENT ASSIGNEE:
Sony Corporation, (214028), 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP), (Applicant designated States: all)
INVENTOR:
MIYAUCHI, Toshiyuki, SONY CORPORATION, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP)
YAMAMOTO, Kouhei, SONY CORPORATION, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP)
LEGAL REPRESENTATIVE:
DeVile, Jonathan Mark, Dr. (91151), D. Young & Co 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1315302 A1 030528 (Basic)
WO 2002019539 020307
APPLICATION (CC, No, Date): EP 2001961290 010831; WO 2001JP7576 010831
PRIORITY (CC, No, Date): JP 2000263120 000831
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H03M-013/29; H03M-013/45
ABSTRACT WORD COUNT: 145
NOTE:
Figure number on first page: 0016

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200322	3842
SPEC A	(English)	200322	98809
Total word count - document A			102651
Total word count - document B			0
Total word count - documents A + B			102651

...SPECIFICATION interleaver 37, uses the received value D29 and a priori probability information D30 to make soft-output decoding of an inner code by making the **MAP decoding** based on the Log-BCJR algorithm. The soft-output decoding circuit 34 generates extrinsic information D31 for information bits determined under code-binding conditions, and...

...soft-output decoding circuit 36.
The soft-output decoding circuit 36 is provided correspondingly to the convolutional encoder 31 in the encoder 1" to make **MAP decoding** based on the Log-BCJR algorithm. The soft-output decoding circuit 36 is supplied with the a priori probability information D32 for code bits of ...

...a priori probability information D33 for information bits whose value is "0", and uses these a priori probability information D32 and D33 to make the **MAP decoding** based ...70 and extrinsic information supplied as a priori probability information from outside or interleaved data EXT (extrinsic information or interleaved data TEXT) to make an **MAP decoding** based on the Log-BCJR algorithm.
At this time, the soft-output decoding circuit 90 makes a decoding operation with a received value type information...M when the value of the data CA exceeds the predetermined value M. The selector 255 supplies data DM obtained via the selection to the **lookup table** 249.
The correction term computation circuit 247 computes the value of a correction term in the log-sum correction. At this time, the correction term...

10/3,K/2 **(Item 2 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

01424782
INTERLEAVING APPARATUS
VERSCHACHTELUNGSVORRICHTUNG
DISPOSITIF D'IMBRICATION
PATENT ASSIGNEE:
Sony Corporation, (214028), 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP), (Applicant designated States: all)
INVENTOR:
Yokokawa, Takashi, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP)
Miyauchi, Toshiyuki, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP)
Yamamoto, Kouhei, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001, (JP)
LEGAL REPRESENTATIVE:
DeVile, Jonathan Mark, Dr. (91151), D. Young & Co 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 1315299 A1 030528 (Basic)
WO 2002019537 020307
APPLICATION (CC, No, Date): EP 2001961288 010831; WO 2001JP7574 010831
PRIORITY (CC, No, Date): JP 2000263134 000831
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H03M-013/27; H03M-013/29; H03M-013/45; H04L-001/00
ABSTRACT WORD COUNT: 167
NOTE:
Figure number on first page: 56

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200322	5032
SPEC A	(English)	200322	99185
Total word count - document A			104217
Total word count - document B			0
Total word count - documents A + B			104217

...SPECIFICATION 70 and extrinsic information supplied as a priori probability information from outside or interleaved data EXT (extrinsic information or interleaved data TEXT) to make an **MAP decoding** based on the Log-BCJR algorithm.
At this time, the soft-output decoding circuit 90 makes a decoding operation with a received value type information...M when the value of the data CA exceeds the predetermined value M. The selector 255 supplies data DM obtained via the selection to the **lookup table** 249.
The correction term computation circuit 247 computes the value of a correction term in the log-sum correction. At this time, the correction term...

10/3,K/3 **(Item 3 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

01402821
Error correction apparatus equipped with turbo decoder
Fehlerkorrekturapparat ausgerustet mit Turbodekoder
Appareil de correction d'erreur equipe de turbo decodeur
PATENT ASSIGNEE:
Kabushiki Kaisha Toshiba, (2077102), 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, (JP), (Applicant designated States: all)
INVENTOR:

Nonin, Katsuya, Int. Prop. Div., K.K.Toshiba, 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105-8001, (JP)
LEGAL REPRESENTATIVE:
HOFFMANN - EITLE (101511), Patent- und Rechtsanwalte Arabellastrasse 4, 81925 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1187340 A2 020313 (Basic)
EP 1187340 A3 030730
APPLICATION (CC, No, Date): EP 2001120647 010830;
PRIORITY (CC, No, Date): JP 2000261574 000830
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H03M-013/29
ABSTRACT WORD COUNT: 97
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200211	320
SPEC A	(English)	200211	2838
Total word count - document A			3158
Total word count - document B			0
Total word count - documents A + B			3158

...CLAIMS generated control signal, so that the received signal has a reverse property of the generated control signal before the received signal is supplied to the **decoding** section of the **turbo decoder** .

3. The error correction apparatus according to claim 1, characterized in that the **turbo decoder** including a calculating section configured to calculate a path metric of the received signal, and an outputting section configured to output a decoding result of the received signal based on the calculated path metric, and a **plurality** of **lookup tables** (509) related to a weighting process executed when calculating the path metric, the lookup tables (509) being switched in accordance with the generated control signal...

...a signal-to-interference ratio (SIR) of the received signal on the basis of the calculated reception power and by the generated control signal, the **turbo decoder** (707) outputting a **decoding** result of the received signal, on the basis of the estimated SIR.

10/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01110804
Statistically multiplexed turbo code decoder
Statistisch multiplexierter Dekoder fur turbokodierung
Decodeur a multiplexage statistique pour turbocodage
PATENT ASSIGNEE:
Nortel Networks Limited, (3029040), World Trade Center of Montreal, 380 St. Antoine Street West, 8th floor, Montreal, Quebec H2Y 3Y4, (CA), (Applicant designated States: all)
INVENTOR:
Freeman, Benedict Russell, 55 Milton Road, Cambridge, CB4 1XA, (GB)
LEGAL REPRESENTATIVE:
Anderson, Angela et al (78508), Nortel Networks Limited IP Law Group London Road, Harlow, Essex CM17 9NA, (GB)
PATENT (CC, No, Kind, Date): EP 973292 A2 000119 (Basic)
EP 973292 A3 021009
APPLICATION (CC, No, Date): EP 99202201 990706;
PRIORITY (CC, No, Date): US 118203 980717
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: H04L-001/00
ABSTRACT WORD COUNT: 192
NOTE:
Figure number on first page: 3

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200003	726
SPEC A	(English)	200003	5967
Total word count - document A			6693
Total word count - document B			0
Total word count - documents A + B			6693

...SPECIFICATION by table 1, for multiplexed packets having a carrier to noise ratio of more than 3 dB to achieve a predetermined bit error rate, a **turbo decoder** should be set for one decode iteration. For multiplex packets having a carrier to noise ratio of between 2.8 and 3dB two **turbo decode** iterations are required, and for packet signals having a carrier to noise ratio of between 2.5 and 2.8dB four **turbo decode** iterations are required. For signals having a carrier to noise ratio of less than 2.5dB, **decoding** of 5 **turbo** code **decode** iterations are required. The analyzer means may store a plurality of look up tables containing data as described above, each of the **plurality** of look **up tables** relating to a **different** value of required bit error rate. The header data includes data identifying an optimum number of iterations of turbo code, generated from the look-up table. Output of demodulator 300 comprises a plurality of packets 302, each having an appended header metrics data 303 describing an optimum number of **turbo** code iterations for **decoding** that particular packet. Each packet output from the demodulator has a different level of associated noise and corruption, and is identified by the metrics header data with an instruction for decoding the packet data.

A key characteristic of a **turbo decode** process, is that the process is iterative. Turbo decoders operate using a plurality of "constituent codes". For example, where two constituent codes are used, the...

10/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01096669
Max-log-APP decoding and related turbo decoding
MAXIMALE LOGARITHMISCHE A-POSTERIORI-WAHRSCHEINLICHKEITSDEKODIERUNG UND ENTSPRECHENDE TURBODEKODIERUNG
Decodage a probabilite a posteriori logarithmique maximale et decodage turbo associe
PATENT ASSIGNEE:
Her Majesty The Queen In Right Of Canada as represented by the Minister of Industry, (2269790), c/o Communications Research Center, 3701 Carling Avenue, P.O. Box 11490, Station H, Ottawa, Ontario K2H 8S2, (CA), (Applicant designated States: all)
INVENTOR:
Crozier, Stewart N., 11 Goulding Crescent, Kanata, Ontario K2K 2N9, (CA)
Hunt, Andrew, 4-371 Nelson Street, Ottawa, Ontario K1N 7S7, (CA)
Gracie, Ken, c/o CRC, 3701 Carling Avenue, Box 11490, Station H, Ottawa, Ontario K2H 8S2, (CA)
Lodge, John, 46 Winchester Drive, Kanata, Ontario K2L 2C9, (CA)
Guinand, Paul, Box 46, 152 Shirreff, Fitzroy Harbour, Ontario K0A 1X0, (CA)
LEGAL REPRESENTATIVE:
Skone James, Robert Edmund (50281), GILL JENNINGS & EVERY Broadgate House 7 Eldon Street, London EC2M 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 963048 A2 991208 (Basic)
EP 963048 A3 010207
APPLICATION (CC, No, Date): EP 99304246 990601;
PRIORITY (CC, No, Date): US 87591 980601

DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H03M-013/00; H03M-013/41
ABSTRACT WORD COUNT: 96
NOTE:
Figure number on first page: 11

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9949	2512
SPEC A	(English)	9949	9974
Total word count - document A			12486
Total word count - document B			0
Total word count - documents A + B			12486

...SPECIFICATION the stopping criterion being satisfied. Here, the Turbo decoder is given a second chance by perturbing the inputs or changing the startup conditions. Preferably, the **Turbo decoding** process is started again using the second set of parity first. Even though the amount of processing is significantly increased for those cases where a second **Turbo decoding** is performed, with the early stopping technique the average amount of processing is only increased slightly at most operating points of interest.

A number of hybrid log-APP/max-log-APP embodiments for performing **Turbo decoding** are also possible. As indicated in the background section, the log-APP decoding algorithm can be implemented using the same max operations as the max-log-APP decoding algorithm, but with an **additional** correction term that can be **looked up** in a **table** . Even through the table lookup approach sounds simple, the required processing is typically about 3 times that of the max-log-APP approaches described above...

...improvement in performance is typically only 0.1 to 0.2 dB, it is still worthwhile for some applications.

An effective hybrid embodiment for performing **Turbo decoding** , that does not require changing the core algorithms themselves, is to use a log-APP decoding algorithm for the first few decoding operations followed by...

10/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00992407
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IE;IT;LI;NL)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire G11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, GLoucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucester GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 897244 A1 990217 (Basic)
APPLICATION (CC, No, Date): EP 98202134 950228;

PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 953013018)
INTERNATIONAL PATENT CLASS: H04N-007/24; G06F-013/00; G06F-009/38;
ABSTRACT WORD COUNT: 120

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9907	298
SPEC A	(English)	9907	126715
Total word count - document A			127013
Total word count - document B			0
Total word count - documents A + B			127013

...SPECIFICATION in a manner described below into a series of input latches (one for each input data signal) collectively referred to as LDIN, which constitute the **secondary** storage elements described above.

In the illustrated example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs...is fifteen bits wide, allowing for parallel transmission of fifteen bits at a time. The value decoder 228 decodes the value image using a first **look - up table** (not shown). A **second** output from the value decode shift register 230 is passed to the value decoder 228 which passes a flag to an index-to-tokens converter...

...be appreciated that bits of other lengths may also be used. The index-to-tokens converter 234 converts the information to token images using a **second look - up table** (not shown) similar to that given in Table 12-3 of the Users Manual. The token images generated by the index-to-tokens converter 234...CODING(underscore)STANDARD token as it flows by the quantizer. When DATA tokens pass thereafter, the inverse quantizer remembers what the standard is and it **looks up** the parameters that it needs to apply to the processing elements in order to perform a proper operation. For example, the inverse quantizer will look ...an interval determined by the register, refresh(underscore)interval.

The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 **decoder** (underscore)clock cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface...

10/3,K/12 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00984065 **Image available**
A PRINTING CARTRIDGE WITH PRESSURE SENSOR ARRAY IDENTIFICATION
CARTOUCHE D'IMPRESSION AVEC IDENTIFICATION D'UNE MATRICE DE CAPTEURS DE PRESSION
Patent Applicant/Assignee:
SILVERBROOK RESEARCH PTY LTD, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SILVERBROOK KIA, Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (Designated only for: US)
Legal Representative:
SILVERBROOK KIA (agent), Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200313861 A1 20030220 (WO 0313861)
Application: WO 2002AU1054 20020806 (PCT/WO AU0201054)
Priority Application: US 2001922207 20010806
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP

KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 142580

Fulltext Availability:
Detailed Description

Detailed Description
... 30,000,000ns). The time taken for 3 color components is 3 times this amount, or 0.09s.

Color Transform
Color transformation is achieved in **two** main ways.

Lookup table replacement
Color space conversion
Lookup Table Rgplacement
As illustrated in Fig. 86, one of the simplest ways to transform the color of a pixel is...s color.

In both cases, the average texture is provided by software, calculated by performing a bi4evel interpolation on a scaled version of the texture **map** . Software determines the next tile's average texture height while the current tile is being applied. Software must also provide the minimum thickness for addition...

10/3,K/13 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00973568 **Image available**
TURBO DECODER WITH MULTIPLE SCALE SELECTIONS
TURBO DECODEUR AVEC DES SELECTIONS MULTI-ECHELLES
Patent Applicant/Assignee:
QUALCOMM INCORPORATED, 5775 Morehouse Drive, San Diego, CA 92121-1714, US , US (Residence), US (Nationality)
Inventor(s):
SHIU Da-shan, 1280 San Tomas Aquino #204, San Jose, CA 95117, US,
SUNDARESAN Rajesh, 3480 Granada Avenue, #270, Santa Clara, CA 95051, US,
Legal Representative:
WADSWORTH Philip R (et al) (agent), Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, California 92121-1714, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200303586 A2 20030109 (WO 0303586)
Application: WO 2002US20345 20020626 (PCT/WO US0220345)
Priority Application: US 2001893046 20010627
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO
RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 9747

Fulltext Availability:
Detailed Description
Claims

Detailed Description
... to a Viterbi decoder, except that there is only one variable (the scaling factors S) since the Viterbi decoder is independent of w.

[00931 - The **Turbo decoder** described herein may be implemented in hardware, software, firmware, or a combination thereof. For a hardware design, the **Turbo decoder** may be implemented within a digital signal processor (DSP), an application specific integrated circuit (ASIC), a processor, a microprocessor, a controller, a microcontroller, a field programmable gate array (FPGA), a programmable logic device, other electronic unit, or any combination thereof. And for a software or firmware design, the **Turbo decoder** may be implemented with codes executed by a processor (e.g., controller 840 in FIG. 8). The storage unit and **lookup tables** may also be implemented with **various** memory technologies such as, for example, random access memory (RAM), dynamic RAM (DRAM), Flash memory, and others. Various structures and implementations of the **Turbo decoder** and storage unit are possible and within the scope of the present invention.

[00941 The foregoing description of the preferred embodiments is provided to enable...

Claim
... wherein the particular number of iterations is less than that required to completely decode the code segment.

4 The method of claim 1, wherein the **decoding** is performed based on a **maximum a posteriori** (**MAP**) **decoding** scheme.

5 The method of claim 4, wherein the **MAP decoding** scheme utilizes a function for decoding the code segment, and wherein the set of one or more parameters includes at least one parameter for the...

...5, wherein the function is a min* function.

7 The method of claim 5, wherein the function is implemented in part with a set of **lookup tables** corresponding to **different** values for the function parameter.
S. The method of claim 1, wherein the set of one or more parameters includes a parameter for a sequence...decoding the code segment, and wherein the constituent decoder and performance metric calculator operate on the code segment for each of the hypotheses.

19 The **Turbo decoder** of claim 18, wherein the constituent **decoder** is a **maximum a posteriori** (**MAP**) **decoder** .

20 The **Turbo decoder** of claim 19, further comprising:
a plurality of lookup tables configured to implement a function for the NIAP decoder, wherein each ...to a particular scale value for the function, and
wherein the plurality of hypotheses correspond to a plurality of scale values to be used for **decoding** the code segment.

21 The **Turbo decoder** of claim 20, wherein the plurality of lookup tables are configured to implement a min* function for the **MAP decoder** .

22 The **Turbo decoder** of claim 18, wherein the bits to be decoded are derived by scaling received bits with a sequence of scaling factors, and wherein the plurality...

10/3,K/14 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00968471 **Image available**
LOW COMPLEXITY CHANNEL DECODERS
DECODEURS DE CANAL A FAIBLE COMPLEXITE
Patent Applicant/Assignee:
INTEL CORPORATION, 2200 Mission College Boulevard, Santa Clara, CA 95052, US, US (Residence), US (Nationality)
Inventor(s):
RAINISH Doron, Kish 3, 52312 Ramat Gan, IL,
YELLIN Daniel, 71 Hertzel Street, 43353 Raannana, IL,
Legal Representative:
HARRIS Scott C (et al) (agent), Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA 92122, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 2002101936 A2-A3 20021219 (WO 02101936)
Application: WO 2002US14878 20020510 (PCT/WO US0214878)
Priority Application: US 2001880707 20010612
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 3577

Fulltext Availability:
Claims

Claim
... the processor's
20 decoding the data packets using the look-up table.

12 The apparatus of claim 10 wherein the processor is configured to **decode** the packet by **turbo decoding** .
. 1
25 13. An apparatus comprising:
14
memory storing a first look-up table with information approximating output of an algorithmic decoding process; and
a the memory stores a
second look - up table with information approximating output of an algorithmic decoding process and wherein the processor is configured to:
(e) interleave the decompressed first result;
(f) compress the...

10/3,K/15 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00939749 **Image available**
WIRELESS COMMUNICATIONS METHODS AND SYSTEMS FOR LONG-CODE AND OTHER SPREAD SPECTRUM WAVEFORM PROCESSING
SYSTEMES ET PROCEDES DE COMMUNICATIONS SANS FIL POUR LE TRAITEMENT DE FORMES D'ONDE A ETALEMENT DU SPECTRE ET DE FORMES D'ONDE LONG CODE
Patent Applicant/Assignee:
MERCURY COMPUTER SYSTEMS INC, 199 Riverneck Road, Chelmsford, MA 01824, US, US (Residence), US (Nationality)
Inventor(s):
OATES John H, 59B Seaverns Bridge Road, Amherst, NH 03031, US,
Legal Representative:
POWSNER David J (et al) (agent), Nutter, McClennen & Fish LLP, One International Place, Boston, MA 02110-2699, US,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200273937 A2-A3 20020919 (WO 0273937)
Application: WO 2002US8106 20020314 (PCT/WO US0208106)
Priority Application: US 2001275846 20010314; US 2001289600 20010507; US 2001295060 20010601
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 149462

Fulltext Availability:
Detailed Description

Detailed Description
... of the processing requirements.

If a particular data user is to be processed with an 80+ ms, latency 804 so as to include the full **turbo** **decode** within the MUD loop then the input channel bit-error rate (BER) pertainI 0 ing to these users might be extraordinarily high. Here, the MUD...

...Each box is the same code but configured differently. The parameters that differ are.
N-FRAMES-RAKE-OUTPUT;
Decoding to be performed (e.g. repetition **decoding** , **turbo** **decoding** , and the like);
Classes of users to be cancelled;
Threshold parameters.

The pseudo code for the software implementation of one long-code multiple user detection...

...physical users
Read
in
rake
outpu@
records (N frames)
Refonnat-rake-output-data (N frames at a time)
for stage = 1 : N-stages
Perform appropriate **decoding** (SRD, **turbo** , and the like, depending on TTI)
Perfon-n-long
code-mud
1 5 end
Free memory
The following four functions are described below.

Read-in-rake-OutpuLrecords;
Reformat-rake-outpuLdata
Perform appropriate **decoding** (SRD, **turbo** , and the like, "depending on TTI);
Perf6nn
long
@code
mud.

The Read-in-rake-output-records function performs.

Reading in data for each user; and...BITS-PER-FRAME-1 150*4.25 640.

Each user class has a specified decoding to be performed. The decoding can be.

None
Soft Repetition **Decoding** (SRD)
Turbo decoding
Convolutional **decoding** .

All **decoding** is Soft-Input Soft-Output (SISO) decoding. For example, an SF 64 voice user produces 600 soft bits per frame. Thus 1,200 soft bits ...and the operation can be performed in-place. If further decoders are included, reduced complexity partial-decode variants can be employed to reduce complexity. For **turbo decoding** , for example, the number of iterations may be limited to a small number.

42
The Long-code MUD performs the following operations.

Respread
Raised-Cosine...a double-buffered lookup table. Values of d and jd are pre-multiplied with beeta by an external processor and stored in a quad-buffered **lookup table** . The alpha calculation state generated the following values for each finger, where subscripts indicate antenna identifier.

0 =pO. (C. AO
jC.j AO)
0C a...

10/3,K/16 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00935279 **Image available**
INTERLEAVER FOR TURBO DECODER
ENTRELACEUR POUR TURBO-DECODEUR
Patent Applicant/Assignee:
QUALCOMM INCORPORATED, 5775 Morehouse Drive, San Diego, CA 92121-1714, US , US (Residence), US (Nationality)
Inventor(s):
YAO Iwen, 5388 Foxhound Way, San Diego, CA 92130, US,
SHIU Da-Shan, 1280 San Tomas Aquino, San Jose, CA 95117, US,
Legal Representative:
WADSWORTH Philip R (et al) (agent), Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200269504 A2-A3 20020906 (WO 0269504)
Application: WO 2002US6030 20020226 (PCT/WO US0206030)
Priority Application: US 2001272123 20010228; US 2001853332 20010510
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 13574

Fulltext Availability:
Detailed Description

Detailed Description
... stored to the proper location (for a write).

[0011] As can be seen, efficient generation of addresses for memory accesses is highly desirable for efficient **Turbo decoding** , especially in light of a complicated interleaving scheme defined by the W-CDMA standard.

SUMMARY
[00121 Aspects of the invention provide techniques to efficiently generate...
...addresses needed to perform interleaving for the Turbo code defined by the W-CDMA standard. In an aspect, to expedite address generation, a number of **lookup tables** (**LUTs**) are provided to store **various** sequences of values used to generate interleaved addresses. The use of these tables expedites address computations and allows the required addresses to be generated in...

...to efficiently generate interleaved addresses based on the tables. The interleaved address generation techniques may be used for Turbo encoding and is especially advantageous for **Turbo decoding** , which is computationally intensive. Expedient address generation is essential for efficient **Turbo decoding** , especially if a high data rate is supported and in light of the iterative nature of **Turbo decoding** .

[00131 A specific embodiment of the invention provides an interleaver for a concatenated convolutional (Turbo) code. The interleaver includes a storage unit, first and second...addresses needed to perform interleaving for the Turbo code defined by the W-CDMA standard. In an aspect, to expedite address generation, a number of **lookup tables** (**LUTs**) are provided to store **various** sequences of values used to generate interleaved addresses. The use of these tables expedites the address computations and allows the required addresses to be generated in less time. The address generation may thus not be the bottleneck for the **Turbo decoding** . Some of these tables and the sequences stored therein are described below.

[00811 In another aspect, techniques are provided herein to efficiently generate addresses based on the tables. The interleaved address generation techniques may be used for Turbo encoding and is especially advantageous for **Turbo decoding** , which is computationally intensive. Expedient address generation is essential for efficient **Turbo decoding** , especially if a high data rate is supported and in light of the iterative nature of Turbo decoding.

[00821 A PRD4E table stores all prime...

10/3,K/17 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00834672
METHOD AND APPARATUS FOR COMPUTING SOFT DECISION INPUT METRICS TO A TURBO DECODER
PROCEDE ET APPAREIL PERMETTANT DE CALCULER DES MESURES DE SORTIE A DECISION PONDEREE POUR UN TURBO DECODEUR
Patent Applicant/Assignee:
QUALCOMM INCORPORATED, 5775 Morehouse Drive, San Diego, CA 92121-1714, US , US (Residence), US (Nationality)
Inventor(s):
SINDHUSHAYANA Nagabhushayana, 7794 Roan Road, San Diego, CA 92129, US,
Legal Representative:
WADSWORTH Philip R (et al) (agent), Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200167617 A2-A3 20010913 (WO 0167617)
Application: WO 2001US7316 20010307 (PCT/WO US0107316)
Priority Application: US 2000521358 20000308
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ

LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG
SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 20134

Fulltext Availability:
Claims

Claim
... the first adder and configured to produce the quotient value, a second adder coupled to the absolute value circuit, a first multiplier coupled to the **second** adder and to the **LUT** , a subtractor coupled to the absolute value circuit, and a second multiplier coupled to the subtractor and to the first multiplier.

39 The device of...

...to a memory element and configured to execute a set of instructions stored in the memory element.
40 A method of estimating log-likelihood (LLR) **decoder** metrics from a **soft decision** having an in-phase component and a quadrature component, the soft decision having been demodulated in accordance with eight@ary phase shift keyed (8PSK) signal...

10/3,K/18 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00811803 **Image available**
VIDEO, AUDIO AND GRAPHICS DECODE, COMPOSITE AND DISPLAY SYSTEM
SYSTEME COMPOSITE DE PRESENTATION A DECODAGE VIDEO AUDIO ET GRAPHIQUE
Patent Applicant/Assignee:
BROADCOM CORPORATION, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
MACINNIS Alexander G, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
TANG Chengfuh Jeffrey, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
XIE Xiaodong, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), CN (Nationality), (Designated only for: US)
KRANAWETTER Greg A, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
HSIUN Vivian, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
CHEUNG Francis, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
BHATIA Sandeep, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), IN (Nationality), (Designated only for: US)
VALMIKI Ramanujan, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), IN (Nationality), (Designated only for: US)
KUMAR Sathish, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
JEON Jun-Young E (agent), Christie, Parker & Hale LLP, Post Office Box 7068, Pasadena, CA 91109-7068, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200145426 A1 20010621 (WO 0145426)
Application: WO 2000US33757 20001213 (PCT/WO US0033757)
Priority Application: US 99170866 19991214; US 2000641374 20000818; US 2000641936 20000818; US 2000643223 20000818; US 2000640870 20000818; US 2000640869 20000818; US 2000641930 20000818; US 2000641935 20000818; US

2000642510 20000818; US 2000642458 20000818
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
((OAPI utility model)) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 85836

Fulltext Availability:
Detailed Description

Detailed Description
... and location on the screen,
allowing the creation of solid color windows with any size and
23
location. Thus, in the preferred embodiment, no pixel **map** is
required, memory bandwidth requirements are reduced and a window
of any size may be displayed.

Another type of graphics window that the window descriptors...memory to
on-chip memory before the graphics window is
displayed.

The system preferably includes a display engine that
processes graphics images formatted in a **plurality** of formats
including a color **look up table** (CLUT) format. The system
provides a data

10/3,K/19 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00543950 **Image available**
FORWARD ERROR CORRECTING SYSTEM WITH ENCODERS CONFIGURED IN PARALLEL AND/OR SERIES
SYSTEME DE CORRECTION AVAL DES ERREURS COMPRENANT DES CODEURS CONFIGURES EN PARALLELE ET/OU EN SERIE
Patent Applicant/Assignee:
VOCAL TECHNOLOGIES LTD,
TORRES Juan Alberto,
DEMJANENKO Victor,
HIRZEL Frederic,
Inventor(s):
TORRES Juan Alberto,
DEMJANENKO Victor,
HIRZEL Frederic,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200007323 A1 20000210 (WO 0007323)
Application: WO 99US17369 19990730 (PCT/WO US9917369)
Priority Application: US 9894629 19980730; US 9898394 19980830; US 99133390 19990510
Designated States: JP US AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 65130

Fulltext Availability:
Detailed Description

Detailed Description
... The concept of Parallel Multiple Concatenated Convolutional Code (PMCCC) utilizes a soft-output decoding and an iterative decoding. We

present two versions of a simplified **maximum a posteriori (MAP) decoding** algorithm. The algorithms work in a sliding window form (like the Viterbi algorithm) and can thus be used to decode continuously transmitted sequences obtained by PMCCC, without requiring code trellis termination. A heuristic explanation is also given of how to embed the **maximum a posteriori** algorithms into the iterative **decoding** of PMCCC. The performances of the two algorithms are compared on the basis of a powerful rate 1/3 PMCCC. Basic circuits to implement the simplified a posteriori decoding algorithm using **lookup tables** , and **two** further approximations (linear and threshold), with a very small penalty, to eliminate the need for lookup tables are proposed.

The broad framework of this analysis...

10/3,K/20 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00336565 **Image available**
SUBTITLING TRANSMISSION SYSTEM
SYSTEME DE TRANSMISSION DE SOUS-TITRES
Patent Applicant/Assignee:
PHILIPS ELECTRONICS N V,
PHILIPS NORDEN AB,
Inventor(s):
VAN DER MEER Jan,
SPIERO Richard Cees,
WEMELSFELDER Armand Victor,
DE HAAN Wiebe,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9619077 A1 19960620
Application: WO 95IB1118 19951212 (PCT/WO IB9501118)
Priority Application: NL 94203642 19941214
Designated States: AU BR CA CN JP KR MX AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 7181

Fulltext Availability:
Detailed Description

Detailed Description
... no& is 9001, coding.M04.eaension is 900"), specifies commands such as map tables and end-of-line indicators which work on the run-length **decoded** data. The concept of **map** tables is disclosed in more details below.

It is envisaged Chat existing On-Screen-Display chips are used for displaying the graphic images. Some of...

...pixel or 8 bits per pixel. A potential problem arises if the pixels within a region are encoded using a number of bits per pixel **different** from the colour- **look - up - table** 's input width. In order to solve this problem, the concept of map tables has been introduced. Map tables also increase the coding efficiency. They...

10/3,K/21 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00334927 **Image available**
CYCLIC TRELLIS CODED MODULATION
MODULATION CYCLIQUE A CODE TREILLIS
Patent Applicant/Assignee:
AT & T WIRELESS SERVICES INC,
Inventor(s):

ALAMOUTI Siavash M,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9617439 A1 19960606
Application: WO 95US15388 19951122 (PCT/WO US9515388)
Priority Application: US 94344111 19941123
Designated States: AL AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TT UA UG UZ VN KE LS MW SD SZ UG AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 1505

Fulltext Availability:
Claims

Claim
... the basis of said determined distances.

27 A receiver as defined in Claim 26, wherein said first and second signal processing circuitry include a Viterbi **decoder** which utilizes **soft - decision** Viterbi **decoding** methods.

28 A receiver as defined in Claim 26, further comprising a constellation signal mapper which maps said received signals to points on said phaselamplitude...

...signal, said trellis decoder comprising: a first look-up table for reconstructing signal constellation points divided into two symmetrical sets of symbol points; and a **second look - up table** for cyclic trellis decoding data mapped according to said signal constellation.

```
File   8:Ei Compendex(R) 1970-2003/Oct W3
         (c) 2003 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2003/Sep
         (c) 2003 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2003/Sep 16
         (c) 2003 EBSCO Publishing
File  65:Inside Conferences 1993-2003/Oct W4
         (c) 2003 BLDSC all rts. reserv.
File   2:INSPEC 1969-2003/Oct W3
         (c) 2003 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2003/Oct W4
         (c)2003 Japan Science and Tech Corp(JST)
File   6:NTIS 1964-2003/Oct W4
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2003/Oct W3
         (c) 2003 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Oct W3
         (c) 2003 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Sep
         (c) 2003 The HW Wilson Co.
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 266:FEDRIP 2003/Sep
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2003/Oct W2
         (c) 2003 FIZ TECHNIK
File 438:Library Lit. & Info. Science 1984-2003/Sep
         (c) 2003 The HW Wilson Co
File  62:SPIN(R) 1975-2003/Sep W2
         (c) 2003 American Institute of Physics
File 239:Mathsci 1940-2003/Dec
         (c) 2003 American Mathematical Society

Set     Items   Description
S1       7549   (SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-
            R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2      16513   (LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3       1121   N(2W)(ENTRY OR ENTRIES)
S4      67884   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
            ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
            OR ASSORT? OR ADDITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5         22   S2(20N)S3:S4
S6          0   S1 AND S5
S7       1287   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
            ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
            OR ASSORT? OR ADDITIONAL)(5N)S2
S8          2   S1 AND S7
S9      26773   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
            ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
            OR ASSORT? OR ADDITIONAL)(5N)TABLE? ?
S10         3   S1 AND S9
S11       637   TABLE? ?(20N)S3:S4
S12         0   S1 AND S11
S13         4?  S8 OR S10
```

13/5/1 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01919817 ORDER NO: AADAA-I1411544
DSP implementation of turbo decoder **using the Modified-Log-** MAP **algorithm**
Author: Khan, Zeeshan Haneef
Degree: M.S.
Year: 2002
Corporate Source/Institution: Florida Atlantic University (0119)
Co-Advisers: Hanqi Zhuang; Raghavan Sudhakar
Source: VOLUME 41/03 of MASTERS ABSTRACTS.
PAGE 833. 134 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544
ISBN: 0-493-91305-X

The design of any communication receiver needs to addresses the issues of operating under the lowest possible signal-to-noise ratio. Among various algorithms that facilitate this objective are those used for iterative decoding of two-dimensional systematic convolutional codes in applications such as spread spectrum communications and Code Division Multiple Access (CDMA) detection. A main theme of any decoding schemes is to approach the Shannon limit in signal-to-noise ratio. All these decoding algorithms have various complexity levels and processing delay issues. Hence, the optimality depends on how they are used in the system. The technique used in various decoding algorithms is termed as iterative decoding. Iterative decoding was first developed as a practical means for **decoding turbo** codes. With the Log-Likelihood algebra, it is shown that a decoder can be developed that accepts soft inputs as <italic>a priori</italic> information and delivers soft outputs consisting of channel information, <italic>a posteriori </italic> information and extrinsic information to subsequent stages of iteration.

Different algorithms such as Soft Output Viterbi Algorithm (SOVA), Maximum A Posteriori (MAP), and Log-MAP are compared and their complexities are analyzed in this thesis. A **turbo decoder** is implemented on the Digital Signal Processing (DSP) chip, TMS320C30 by Texas Instruments using a Modified-Log-MAP algorithm. For the Modified-Log-MAP-Algorithm, the optimal choice of the lookup table (**LUT**) is analyzed by experimenting with **different LUT** approximations. A low complexity decoder is proposed for a (7,5) code and implemented in the DSP chip. Performance of the decoder is verified under the Additive Wide Gaussian Noise (AWGN) environment. Hardware issues such as memory requirements and processing time are addressed for the chosen decoding scheme. Test results of the bit error rate (BER) performance are presented for a fixed number of frames and iterations.

13/5/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1962201 NTIS Accession Number: N96-25256/4
Soft-Output Decoding **Algorithms in Iterative** Decoding **of** Turbo **Codes**
Benedetto, S. ; Montorsi, G. ; Divsalar, D. ; Pollara, F.
Jet Propulsion Lab., Pasadena, CA.
Corp. Source Codes: 014828000; JJ574450
Sponsor: National Aeronautics and Space Administration, Washington, DC.
15 Feb 96 25p
Languages: English Document Type: Journal article
Journal Announcement: GRAI9619; STAR3409
In Its the Telecommunications and Data Acquisition Report p 63-87.
NTIS Prices: (Order as N96-25250, PC A10/MF A02)
Country of Publication: United States
In this article, we present two versions of a simplified **maximum a posteriori decoding** algorithm. The algorithms work in a sliding window

form, like the Viterbi algorithm, and can thus be used to decode continuously transmitted sequences obtained by parallel concatenated codes, without requiring code trellis termination. A heuristic explanation is also given of how to embed the **maximum a posteriori** algorithms into the iterative **decoding** of parallel concatenated codes (**turbo** codes). The performances of the two algorithms are compared on the basis of a powerful rate 1/3 parallel concatenated code. Basic circuits to implement the simplified a posteriori decoding algorithm using **lookup tables** , and **two** further approximations (linear and threshold), with a very small penalty, to eliminate the need for lookup tables are proposed.

Descriptors: *Concatenated codes; *Data transmission; *Decoding; *Iterative solution; Parallel processing (Computers); Trellis coding

Identifiers: *Foreign technology; Reprints; NTISNASA

Section Headings: 45G (Communication--Communication and Information Theory)

13/5/3 (Item 2 from file: 6)

DIALOG(R)File 6:NTIS

1292869 NTIS Accession Number: AD-A177 823/2

Frequency Hopped M-arcy Frequency Shift Keyed Communications Using List Metric Decoding Over Jamming and Multiple Access Channels

(Doctoral thesis)

Creighton, M. A.

California Univ., Los Angeles.

Corp. Source Codes: 005420000; 072250

1986 387p

Languages: English Document Type: Thesis

Journal Announcement: GRAI8712

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A17/MF A01

Country of Publication: United States

List metric decoding is applied to anti-jam and multiple access communication systems that employ frequency-hopped, M-ary Frequency Shift Keyed (MFSK) modulation. The performance of these systems over Guassian noise and Rayleigh fading channels is analyzed by deriving expressions for the cutoff rate parameter RO, and evaluating numerical examples. RO represents the largest reliable data rate per coded symbol that could be achieved, with a particular system and channel, by using practical coding methods. Because it is code-independent, RO is used as the basis for comparing list **decoding** against hard and **soft decisions** , without the encumbrance of analyzing specific error correcting codes. RO is then used later, along with a code-dependent function, to upper bound the bit error probability provided by a particular code. In a list decoding receiver, decisions are based on the relative magnitudes of the demodulator's energy detector outputs.

Descriptors: Antijamming; *Coding; *Decoding; *Demodulators; *Communication and radio systems; Channels; Detectors; Decision making; Receivers; Errors; Probability; **Tables** (Data); **Multiple** access; Symbols; Output; Energy; Hardening; Rates; Data rate; Reliability; Fading(Electromagnetic waves); Error correction codes; Modulation

Identifiers: Theses; NTISDODXA

Section Headings: 45C (Communication--Common Carrier and Satellite); 63B (Detection and Countermeasures--Electromagnetic and Acoustic Countermeasures); 45G (Communication--Communication and Information Theory)

13/5/4 (Item 1 from file: 239)

DIALOG(R)File 239:Mathsci

02426092 MR 94c#94009

Error correcting codes.

Theory and applications. With a preface by G. Cullmann. Translated from the 1989 French original by Iain Craig.

Poli, Alain (UER Mathematiques, Informatique, Gestion (MIG), Universite de Toulouse III (Paul Sabatier), 31062 Toulouse, France)
Huguet, Llorenc
Contributors: Craig, Iain; Cullmann, G.
Corporate Source Codes: F-TOUL3
Publ: Prentice Hall International, Hemel Hempstead; Masson, Paris, 1992, xvi+512 pp. ISBN: 0-13-284894-5
Language: English Summary Language: English
Document Type: Book
Journal Announcement: 9308
Subfile: MR (Mathematical Reviews) AMS
Abstract Length: LONG (57 lines)

The preface states that the purpose of this book is to collect in one volume some of the questions discussed at the AAECC conferences held during the 1980s in Europe (with one conference in Japan). This book has a half dozen or so authors who wrote various chapters or portions of chapters. Poli and Huguet wrote the most. This arrangement is noticeable and leads to a lack of coherence among the chapters.

A listing of the chapters and some of their contents follows: 1. Information theory; 2. Elements of algebra: includes vector spaces, some polynomial rings, group characters, Hadamard matrices and Krawtchouk polynomials; 3. Finite fields: includes the usual properties and some computational topics; 4. Classical error-correcting codes: many of the standard properties of binary codes, MacWilliams equations, cyclic codes, BCH codes, R-S and other classic codes; 5. Further algebra: includes multivariable codes, modular codes and Grobner bases; 6. Other error-correcting codes: includes more on multivariable codes, product codes, codes over rings, algebraic geometry codes; 7. Codes and combinatorics: includes standard bounds, t-designs and codes, association schemes; 8. Application of codes: includes maximum likelihood **decoding** , **soft - decision decoding** and some implementations; 9. **Tables** and curves: includes **various tables** related to computing in finite fields and performance curves.

This is not an easy book to read for many reasons. The first three chapters are included because they provide material useful for understanding codes and their uses. While this is true, until one reaches page 156 (Chapter 4), block codes are not even defined. Without motivation these chapters can be rather dry reading. Chapter 4 treats only binary codes, saying the generalization to other finite fields is easy. This is really not so in many situations. A book which covers so many areas in coding should give the basic results over an arbitrary finite field. There are examples through much of the volume but not enough for someone to learn all the material covered in this book. The volume is translated from the French and the reader is aware of this in many instances. An example of this is the heading for Section 3.1: Every finite field is commutative. The usual definition of a field is a commutative skew field. Perhaps skew field is translated as field. There are other unfamiliar terms: control matrix for parity-check matrix. In a book like this with so many topics and so many authors, a comprehensive index would be a great help. In fact, the index is quite minimal. I could not find most of the terms I looked up. Much searching failed to find any definition of auto-dual codes. More surprising is the absence of covering radius in the index or any definition or discussion of this important topic anywhere that I could see, although a few results are mentioned in Chapter 7. Also strange was the absence of a findable definition of convolutional codes even though their performances compared to block codes are mentioned in Chapter 8.

As these remarks indicate, I think this book will be most useful to someone already working in coding who would like to find out more about some of the topics, many quite current, mentioned in the chapter list. Most of the newer areas are in the last half of the book. It is also possible that mathematicians interested in applications can find them here.

Reviewer: Pless, Vera (1-ILCC)
Review Type: Signed review
Descriptors: *94Bxx -Information and communication, circuits-Theory of error-correcting codes ; 94-02 -Information and communication, circuits-Research exposition (monographs, survey articles)

```
File 275:Gale Group Computer DB(TM) 1983-2003/Oct 28
         (c) 2003 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2003/Oct 29
         (c) 2003 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2003/Oct 28
         (c) 2003 The Gale Group
File  16:Gale Group PROMT(R) 1990-2003/Oct 28
         (c) 2003 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2003/Oct 28
         (c)2003 The Gale Group
File 624:McGraw-Hill Publications 1985-2003/Oct 29
         (c) 2003 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2003/Oct 29
         (c) 2003 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2003/Sep W3
         (c) 2003 CMP Media, LLC
File 674:Computer News Fulltext 1989-2003/Oct W4
         (c) 2003 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2003/Oct 27
         (c) 2003 The Dialog Corp.
File 369:New Scientist 1994-2003/Oct W3
         (c) 2003 Reed Business Information Ltd.

Set     Items   Description
S1        477   (SOFT()DECISION? ? OR MAP OR (MAX OR MAXIM?)(3W)(APOSTERIO-
                 R? OR A()POSTERIOR?) OR TURBO)(5N)DECOD?
S2       9068   (LOOKUP? ? OR LOOK???()UP)(3N)TABLE? ? OR LUT OR LUTS
S3        638   N(2W)(ENTRY OR ENTRIES)
S4      57714   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
                 ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
                 OR ASSORT? OR ADDITIONAL)(5N)(INDEX??? OR INDICE? ?)
S5          32   S2(20N)S3:S4
S6           0   S1 AND S5
S7         899   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
                 ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
                 OR ASSORT? OR ADDITIONAL)(5N)S2
S8           4   S1 AND S7
S9       67151   (SECOND? OR TWO OR 2ND OR DUAL? OR MULTIPLE OR MULTIPLICIT-
                 ??? OR PLURAL? OR SEVERAL OR VARIOUS OR DIFFERENT OR SEPARATE
                 OR ASSORT? OR ADDITIONAL)(5W)TABLE? ?
S10          4   S1 AND S9
S11       3025   TABLE? ?(20N)S3:S4
S12          0   S1 AND S11
S13          8   S8 OR S10
S14          4   RD (unique items)
```

14/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02389120 SUPPLIER NUMBER: 61415741 (USE FORMAT 7 OR 9 FOR FULL TEXT)
FPGAs cranked for software radio.(Technology Information)
Dick, Chris
Electronic Engineering Times, 112
April 10, 2000
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1850 LINE COUNT: 00156

... software-defined radio performs many sophisticated signal-processing tasks, including advanced compression algorithms, power control, channel estimation, equalization, forward error control (Viterbi, Reed-Solomon and **turbo** coding/ **decoding**) and protocol management.
Digital filters are employed in a number of ways in DSP-based transmitters and receivers. Polyphase interpolators are used in the transmitter...

...streams. As a specific example, consider the Xilinx Virtex series of FPGAs. The logic elements, called slices, essentially consist of a pair of four-input **lookup tables** (**LUTs**), **several** multiplexers and some **additional** silicon support that allows the efficient implementation of carry-chains for building high-speed adders, subtracters and shift registers. Two slices form a configurable-logic...

14/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01673744 SUPPLIER NUMBER: 15092145 (USE FORMAT 7 OR 9 FOR FULL TEXT)
NexGen enters market with 66-MHz Nx586; first Pentium competitor uses RISC-like core and optional FPU. (Nx586 features Reduced Instruction Set Computer-like core and Floating Point Unit) (includes related article on pricing and availability of the Nx586 chip) (Product Announcement)
Gwennap, Linley
Microprocessor Report, v8, n4, p12(6)
March 28, 1994
DOCUMENT TYPE: Product Announcement ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4825 LINE COUNT: 00371

... mem], CX translates into three RISC86 instructions:
LOAD R2, [R1]
ADD R2, R3
STORE [R1], R2
where the physical register numbers are assigned by the **decoder** to **map** the x86 registers appropriately.
Iterative x86 string instructions translate into an indefinitely long sequence of internal instructions. The decoder issues RISC86 instructions as fast as...same time and in much the same way as the other three function units. The FPU can execute double-precision adds and multiplies in just **two** cycles, one fewer than Pentium; **Table** 1 shows the latencies for various math operations. NexGen did not implement Pentium's parallel FXCH feature and thus chose not to pipeline the FPU...to predict branches. According to the patent, each BPC entry contains two prediction bits. If a branch misses the BPC, an additional 2,048-entry, **two** -bit-wide branch history **table** is checked, increasing the predication accuracy compared with Pentium's 256-entry branch target buffer.
Although these two structures will correctly predict most conditional branches...

14/3,K/3 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07808472 Supplier Number: 65077325 (USE FORMAT 7 FOR FULLTEXT)
Use Forward Error Correction To Improve Data Communications. (Technology Information) (Tutorial)
Hewitt, Eric; Thesling, William H.
Electronic Design, v48, n17, p111
August 21, 2000
Language: English Record Type: Fulltext Abstract
Article Type: Tutorial
Document Type: Magazine/Journal; Trade
Word Count: 3628

... that a given bit is a logical 0 is related to this number. These metrics are usually represented by 3- or 4-bit integers called **soft decision** metrics. The **decoder** output is an estimate of the k information bits. Typically, **decoding** with **soft decision** metrics is computationally intensive. Very often, it's performed on a decoder ASIC that's specifically designed for the task.

A code's performance is...as per encoder 2 and the second decoding is as per encoder 1. Between the two decodings, the scrambling operation is reversed.

What makes a **Turbo** Code unique is that the **decoding** process can be performed again. The second constituent decoder addresses errors left from the first. The second pass of the first decoder then addresses errors ...

...the other decoder. In order to maximize performance, this decoding process is typically iterated several times.

For this iterative process to work optimally, each constituent **decoder** must take **soft decision** metrics as its input in addition to generating soft outputs. Every decoder has to generate an output of n soft decision metrics corresponding to the...

...a high-performance engine. The turbocharger uses engine exhaust (output) to power an air intake blower, thus enhancing the input. This is where the term " **turbo** "in **Turbo** Code comes from. **Turbo** codes are iteratively **decoded** codes.

Turbo Code technology can best be illustrated with an example that uses block codes as the constituent codes. Consider the (8,4) extended Hamming code of...study, because this floor limits the use of TCCs in many systems.

TCCs and TPCs have slightly different properties which makes them well-suited for **different** applications. The **table** in this article can serve as a guide.

The performance Turbo Codes can achieve guarantees that they are here to stay. As more communication system...

14/3,K/4 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01213207 CMP ACCESSION NUMBER: EET20000410S0080
FPGAs cranked for software radio
Chris Dick, Senior System Engineer, Manager, Signal Processing Team, Xilinx Inc., San Jose, Calif.
ELECTRONIC ENGINEERING TIMES, 2000, n 1108, PG112
PUBLICATION DATE: 000410
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Signals - Focus: DSP World, Cores
WORD COUNT: 1690

... software-defined radio performs many sophisticated signal-processing tasks, including advanced compression algorithms, power control, channel estimation, equalization, forward error control (Viterbi, Reed-Solomon and **turbo** coding/ **decoding**) and protocol management.

Digital filters are employed in a number of ways in DSP-based transmitters and receivers. Polyphase interpolators are used in the transmitter...

...streams. As a specific example, consider the Xilinx Virtex series of FPGAs. The logic elements, called slices, essentially consist of a pair of four- input **lookup tables** (**LUTs**), **several** multiplexers and some **additional** silicon support that allows the efficient implementation of carry- chains for building high-speed adders, subtracters and shift registers. Two slices form a configurable-logic...